

HiFive1 Rev B Schematics

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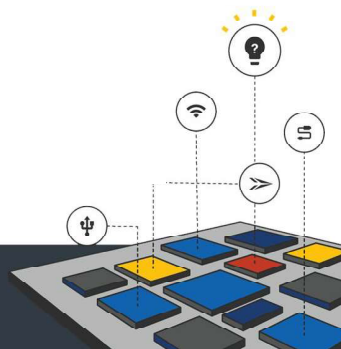
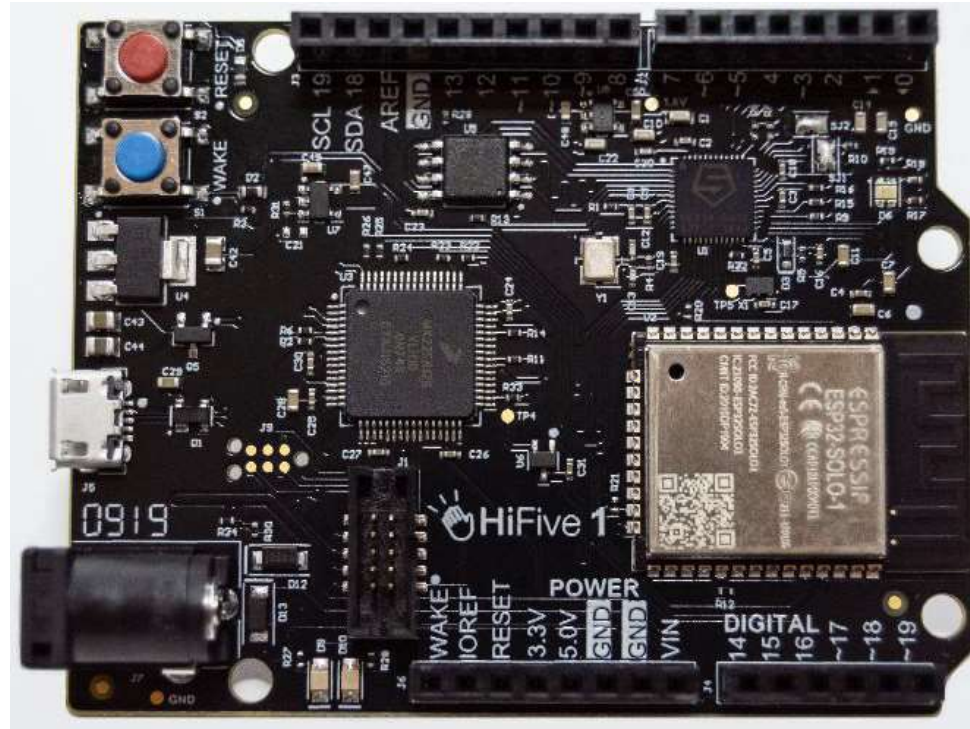
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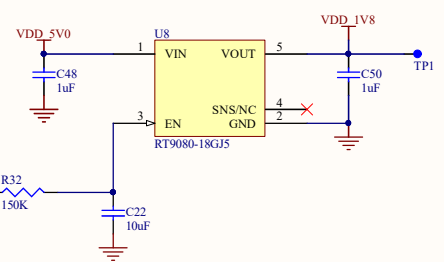
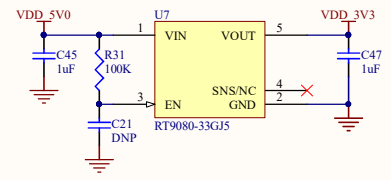
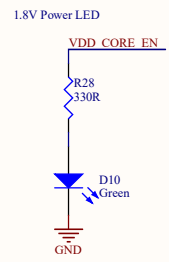
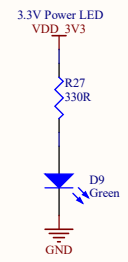
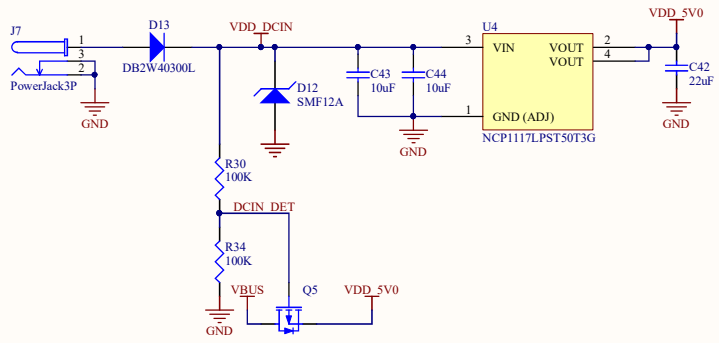
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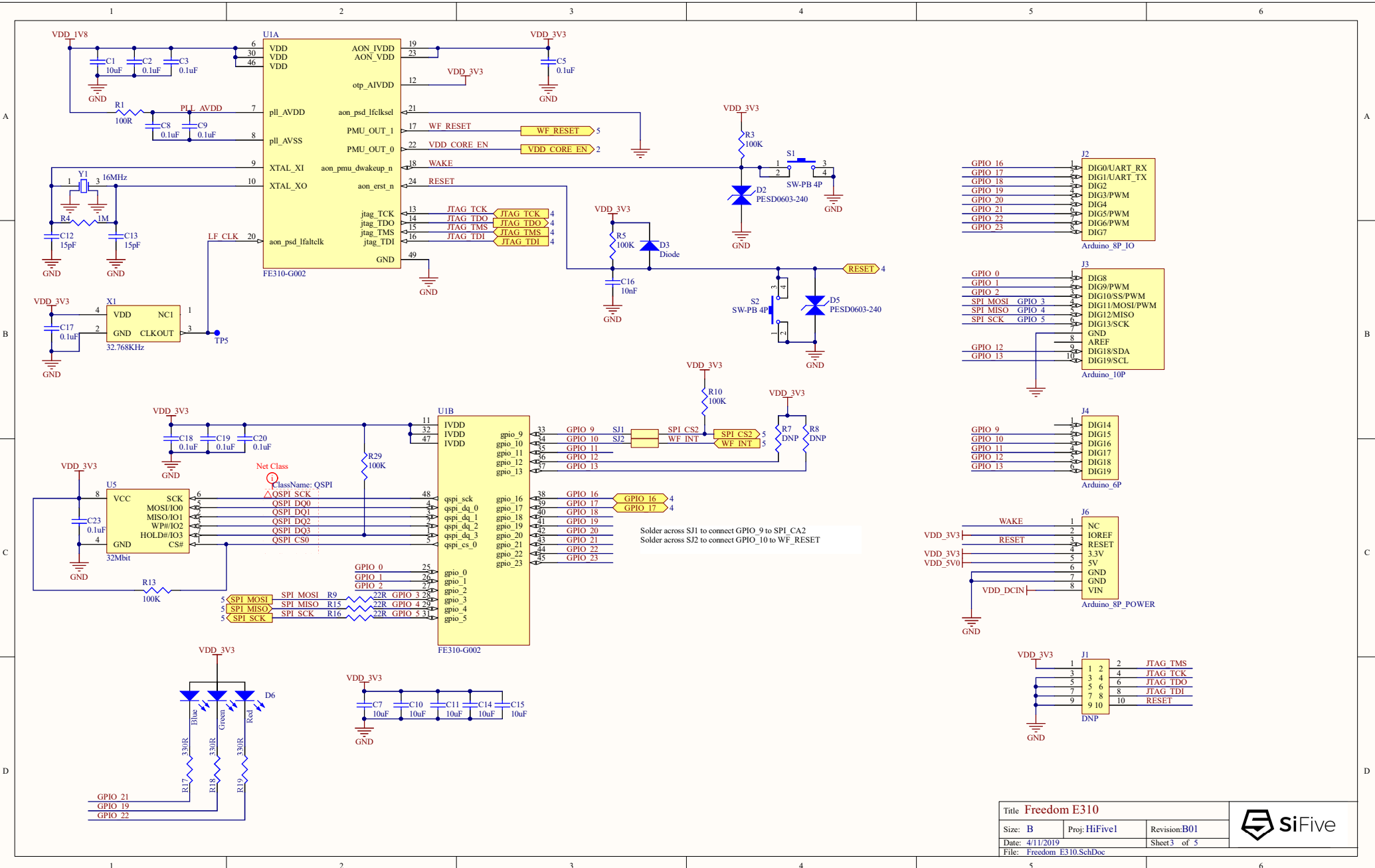
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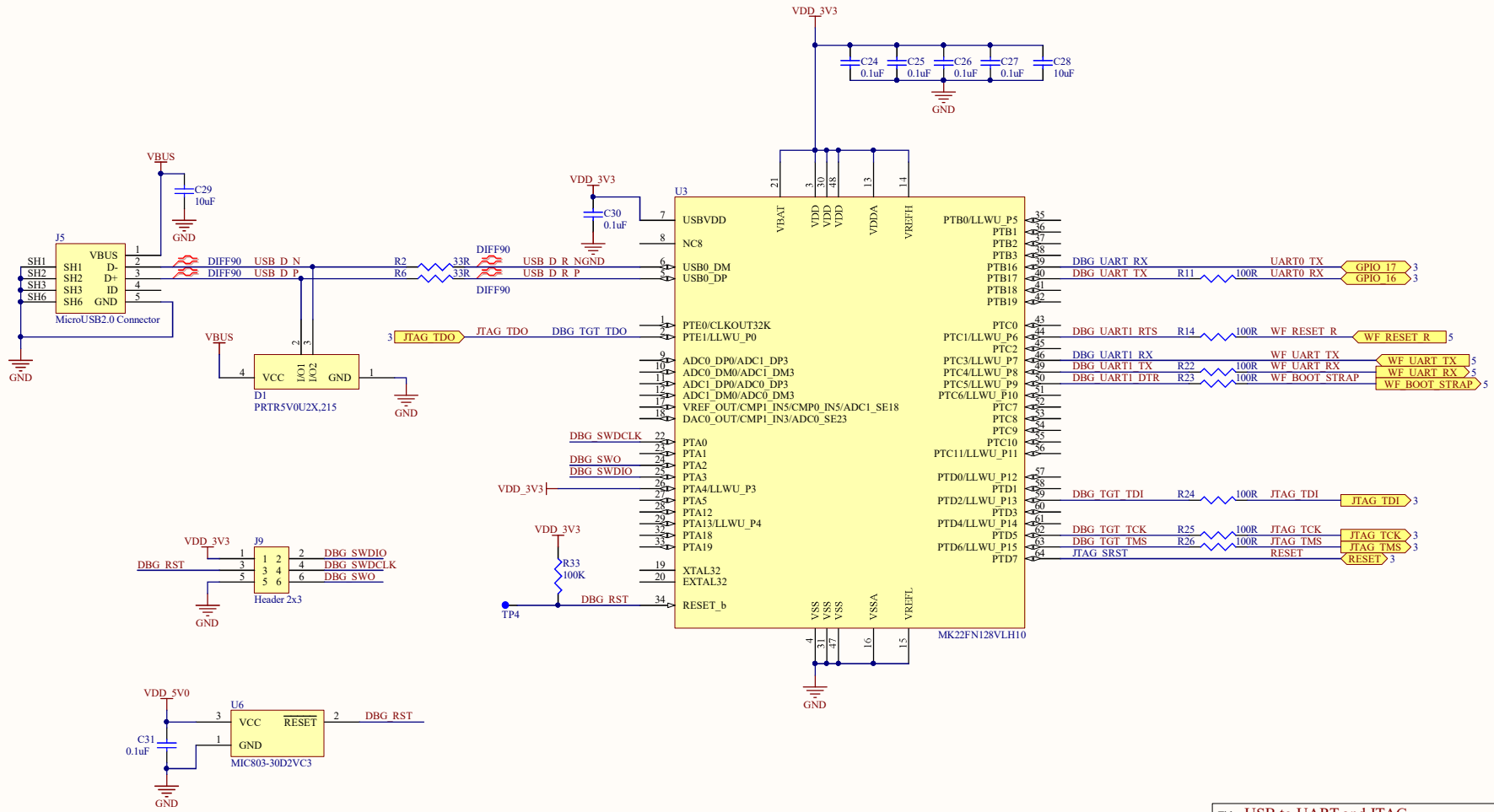
HiFive 1 Rev B01



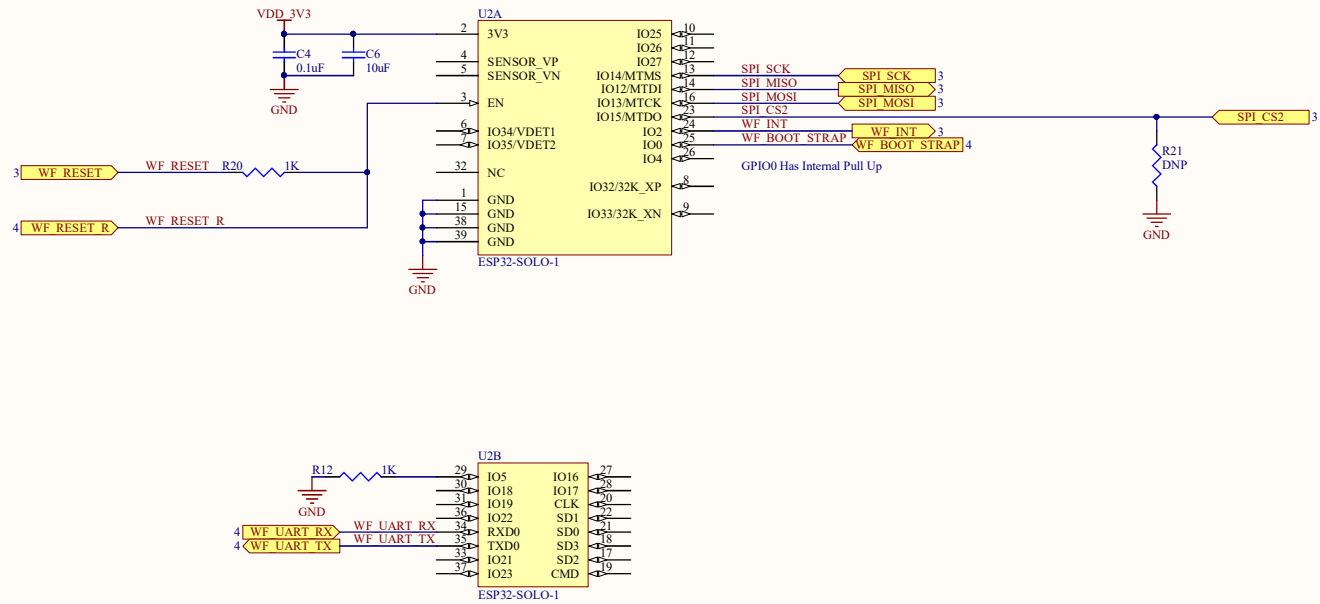


| | | | |
|---------------------------|---------------|---------------|--|
| Title Power Supply | | | |
| Size: B | Proj: HiFive1 | Revision: B01 | |
| Date: 4/1/2019 | Sheet2 of 5 | | |
| File: Power.SchDoc | | | |





| | | | |
|----------------------------|---------------|---------------|--|
| Title USB to UART and JTAG | | | |
| Size: B | Proj: HiFive1 | Revision: B01 | |
| Date: 4/1/2019 | Sheet4 of 5 | | |
| File: Debug.SchDoc | | | |



Timing of SDIO Slave Boot Strap

| Pin | Default | Falling-edge Input | Falling-edge Output | Rising-edge Input | Rising-edge Output |
|-------|------------------|--------------------|---------------------|-------------------|--------------------|
| | | 0 | 1 | 0 | 1 |
| MTDO | Internal Pull-up | 0 | 0 | 1 | 1 |
| GPIO5 | Internal Pull-up | 0 | 1 | 0 | 1 |