StarFive 赛昉科技

JH7100
Datasheet

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About This Manual

Introduction

StarFive JH7100 is an AI vision and image processing platform based on RISC-V. This document mainly provides the users with technical specifications of JH7100.

This release is intended for evaluation purposes only.

Revision History

Version	Released	Revision
V1	2021-09-30	First release for VisionFive.

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1 Introduction

Equipped with dual-core U74, JH7100 shares 2MB of L2 cache and supports Linux OS. The StarFive ISP is compatible with mainstream camera sensors and the built-in image/video processing subsystem supports H265/H264/JPEG codec. With high-performance, low-power Vision DSP and NNE integrated, JH7100 will make thinking more intelligent and efficient. JH7100 can meet the various real-time visual processing needs of the edge end thanks to the capabilities of various complex image/video processing and intelligent visual calculations.

1.1 Highlighted Features

The highlighted features are list as follows:

- RISC-V U74 Dual core with 2MB L2 cache, support Linux; 1.0GHz
- Vision DSP Tensilica-VP6 for computing vision
- NVDLA Engine 1 core (configuration 2048 MACs@800MHz)
- Neural Network Engine (1024MACs@500MHz)
- 2xchannels of 32bit LPDDR4/DDR4, 3200Mbps(25.6GB/s), high efficiency required
- Video Decoder(H264/H265): up to 1 channel 4K@60fps or 8 channel 1080p30fps
- Video Encoder(H264/H265): up to 1 channel 4K@60fps or 8 channel 1080p30fps
- Dual channels of ISP, each channel support up to 4K@30fps
- Support up to 3 video input, 1x for DVP and 2x for MIPI-CSI with 4D2C up to 4K@30fps
- Support LCD or MIPI-DSI output up to 4K@30fps
- Support MIPI-CSI TX for video output after ISP and AI processing
- JPEG Encoder/Decoder up to 8M@30fps
- USB3.0/2.0 Host/Device mode
- Support 1000Mbps Ethernet MAC
- Support TRNG and OTP
- Support DMAC, QSPI and other peripheral
- Dedicated Audio Processing DSP and sub-system

2 Features

2.1 CPU Subsystem

2.1.1 Overview

- 64-bit High performance RISC-V CPU (U74) Dual cores for main general computing
- 32bit RISC-V CPU core (E24) for low power and real control/configure tasks as co-processor
- L2-cache up to 2MB cache size
- Easy Master (EZMAST) works as event co-processor for high efferent events handling
- Dual DMA controller for memory-to-memory and memory-to-peripheral data exchange
- Support Linux/VxWorks/RTOS

2.1.2 SiFive U74 Dual Core

- Fully-compliant with the RISC-V ISA specification
- Dual-core with Cache coherence
- RV64GFC U74 Application Core, each core has
  - 32KB L1 I-cache with ECC (8-way)
  - 32KB L1 D-cache with ECC (8-way)
  - 8 Region Physical Memory Protection
  - Embedded MMU support Linux OS
  - Sv39 Virtual Memory support with 38 Physical Address bits
  - PMP with 8 regions and a minimum granularity of 4096 bytes.
- CLINT for timer and software interrupts
- PLIC with support for up to 127 interrupts with 7 priority levels
- Support SCIE (SiFive Customer Inst Extension)
- Support JTAG as Debug port
- Support Multiple AXI Interface including system, peripheral, memory port and front port

2.1.3 SiFive E24 Core

- Fully-compliant with the RISC-V 32 ISA specification
- RV32IMAFC E24 Core
  - 16KB I-cache with 32 Byte cache line
  - 64KB TIM with two banks and atomic operation
  - 4 Region Physical Memory Protection
- CLIC with support for up to 127 interrupts with 16 priority levels
- Support JTAG as Debug port

- Support AHB-Lite system bus for2GB memory map

2.1.4 EZMAST

- AHB master and AHB slave port
- When CPU power down, it can operate bus through event trig
- Support 128 events
- 25 opcode

2.1.5 DMA

- Support general DMA operation and Scatter Gather DMA
- Support up to 16+4 channels
- Support up to 32 requests, the detail configured request number is TBD
- Support AXI4 bus interface
- Support AXI Bus width of 64/128 bits
- Support memory to memory, memory to peripheral, peripheral to memory and peripheral to peripheral transfer
- Transfer complete interrupts and error interrupts are generated
- Arbitration supported - fixed and round robin
- Provides Status of each transfer through status register for each channel
- Support 4+4 Scatter Gather channels in all 16+4 channels

2.2 Memory and Storage

2.2.1 On Chip Memory

- BUS RAM up to 256KB
- Shared BUS memory with DLA 2MB
- Boot ROM up to 32KB

2.2.2 DDR

- DDR controller
  - Support 2 channel of x32
  - DDR4/3 and LPDDR4/3 modes & signaling, rates up to following speed:
    - 2133Mbps (DDR3/LPDDR3)
    - 3200 Mbps (DDR4/LPDDR4)
  - Internal de-skew PLLs for high speed, low jitter clock generation (clk4x)
  - x16/x32 data path interface extendable
  - DRAM ranks of 1, 2 (could be asymmetric)
  - Bank-interleaving & rank-interleaving (symmetric ranks only)

- Support for dynamic DRAM frequency scaling
- Automated clock gating of internal logics
- Error-correction code (SECDED) to select DRAM memory space
- Address region-based security control support
- Automated low power control of DRAM devices
- AMBA AXI4 protocol for main data path interface for DDR controller
- AMBA APB4 protocol for configuration register access interface for DDR controller
- Flexible refresh control
  - Automated adjustment of refresh interval
  - Pulled-in or postponed of refreshes
  - Dynamic per-bank / all-bank refresh switching
  - Opportunistic advanced per-bank refresh
- Open page based advanced page policy
  - Programmable timeout pre-charge
  - Auto pre-charge for reducing command congestion
- Independent read and write timing adjustments with auto calibration
- Various power-down modes for low power including self-refresh support
- DFI 4.0 specification between DDR controller and DDR PHY

■ DDR PHY

- High resolution write/read timing control
- Per-bit de-skew on the write data path
- Per-bit de-skew on the read data path
- Support for multiple leveling/training modes through PHY evaluation mode
- Register programming interface to all PHY parameters
- PHY independent mode training logic
- Write/read data timing per-chip select
- Low-power modes
- Low-speed test interface (PHY BIST)
- At-speed ATPG support (OPCG)
- DBI support
- PHY controller frequency ratio of 2:1
- IO calibration
- JTAG interface
- Boundary scan support
- Testability features

2.2.3 QSPI

- QSPI master controller
- Programmable master mode
- Data rate up to 100M bps per bit
- 1/2/4 data bit
- Support XIP mode and Boot mode
- Separate data input and output bit

2.3 Vision and AI Computing

2.3.1 VP6

- Highly efficient 32-bit base architecture
- Extend with designer-defined, application-specific instructions, execution units, register files, and I/Os
- 7-stage pipeline depth for core instruction set architecture (ISA)
- Histogram operations
- Up to 32 interrupts
- Local memories configurable up to 256KB ITCM and 256KB DTCM
- 32KB instruction Cache
- Up to 128b-wide flexible-length instruction extensions (FLIX) instructions
- Multi-core on-chip debug (OCD) with break-in/break-out
- Dual-load/stores each up to wide with data cache support and multi-bank RAM support
- Compatible interfaces for ARM® CoreSight™ debug and trace technology
- IEEE 754-compliant single-/double-precision scalar floating-point unit
- 1 AXI Master port and 1 AXI Slave port
- single-channel integrated DMA engine
- Complete matching software development tool chain
- Support generic RTOS Compatibility

2.3.2 DLA

- NVDLA based
- High-performance convolution core with 2048 MACs
- Support various image input formats
- Dedicated Depth-wise Convolution engine
- Acceleration engine for Activation functions
- Acceleration engine for Pooling

- Acceleration engine for advanced Normalization functions
- Memory-to-memory transformation acceleration for tensor reshape and copy operations
- 2MB local on-chip SRAM, shared by AXI slave port accessed by other BUS master

2.3.3 NNE50

- Input feature map size (Width x Height): No Limited
- Precision: INT8
- Normal and Depth-wise Convolution Operations
- Non-normal Convolution Operations (such as transposed convolution, dilated convolution)
- Pooling Operations
  - Average Pooling, and Maximum Pooling Algorithm
  - Size (Width x Height): 2x2, 4x4
- Element-wise Operations
  - Element-wise addition, and multiplication are both support
- Activation Operations
  - ReLU, LeaklyReLU, LReLU, Tanh, Sigmoid, and other types of non-linear activation functions are all supported
- Fully-Connected Operations
  - There is no limit on input feature map size, however, large connections might degrade NNE50 performance because of the restriction of on-chip SRAM size
- Shortcut Operations
  - Currently only 1 frame shortcut is support.
- Batch Normalization are support.

2.3.4 VAD

- Ultra-low power Voice Activity Detector for audio bit-stream as a Voice Trigger
- Speaker/Silence detection; Data buffering wrapped for command recognition
- Configurable multi-channel (1-4) support both output of ADC(AMIC) and PDM(DMIC)
- Support 16KHz sample rate; 16-bit precision
- Up to 128K bytes ring buffer reload address can be configured by software

2.4 Video Processing Subsystem

2.4.1 Camera MIPI IN/OUT Interface

- CSI-2 RX Controller
  - Support of the MIPI CSI-2 v1.3 protocol over D-PHY PPI interface up to maximum 4*1.5Gbps
  - Pixel interface supporting
  - Byte to pixel conversion one-pixel interface
  - Direct memory dump using packed byte operation

  - Flow control
  - Payload FIFO operation
  - Monitoring of frame for automatic start/end of frame synchronization when enable
  - Extended Functions for Virtual Channel extension and RAW16/20 modes as defined for MIPI CSI-2 V2.0 Specification
  - Enable by setting v2p0_support_enable bit in the static_cfg configuration register
  - RAW16/RAW20 become valid data types
  - VCX (Virtual Channel Extension) will be employed - Effects ECC handing
- MIPI RX D-PHY
  - Support standard 8b PPI interface compliant of MIPI D-PHY spec
  - Support total up to 6 lanes in D-PHY and data rate up to 1.5Gbps
  - Support 1 clock Lane and up to 4 Data Lane scalability in DPHY mode
  - Support independent (1 Clock Lane and up to 2 Data lanes) x2 in DPHY mode
  - Support lane swap in MIPI D-PHY configuration for convenient package and PCB board routing
  - Support clock and data lane swapping function
  - Support Triggers, ULPS and LPDT
- CSI-2 TX Controller
  - CSI-2 Protocol handling
  - CSI-2 interface up to a maximum of four 2.5Gbps data lanes
  - High Speed data transmission
  - Automatic LP control for clock and data lane power saving
  - Automatic synchronization short packets generation (frame start, frame end, line start, line end)
  - Automatic frame counting when enabled
  - Automatic line counting when enabled
  - Pixel byte-to-packet conversion
  - Virtual Channel/Data type interleaving
  - Protocol error detection
  - Interrupt generation
  - Bypass mode
  - Share MIPI TX DPHY with DSI controller

2.4.2 ISP

- Sensor Interface
  - Support up to 4K (3840x2160) pixels @30fps CMOS RGGB image sensor
  - Support one MIPI and one DVP sensor input interface
  - Support 12-bit sensor data input
- Image processing engine
  - Built-in color pattern generation

  - Sensor black level compensation
  - Defective pixel correction
  - R/G/B LUT for sensor linearization correction
  - Image analysis for AE, AWB and AF
  - Programmable histogram analysis
  - White balance control
  - Lens shading compensation
  - Color shading compensation
  - CMOS sensor spatial crosstalk cancellation (Gr and Gb balance filter)
  - Advanced Bayer CFA color interpolation
  - False color suppression
  - Advanced edge control and enhancement
  - R/G/B Gamma LUT
  - Color correction matrix
  - Color space conversion
  - Brightness/contrast and hue/saturation adjustment
  - Global tone mapping
  - Spatial noise reduction
- Back end processing
  - Seamless digital scale down from 1/4x to 1x
  - Support up to 3 channel video streaming

2.4.3 Video Encoder

- 4K 60frames X1 channel/sec or 1080p 30frames X8 channel/sec @ 500Mhz
- H.265/HEVC Encoder
  - Fully compatible with ISO/IEC 23008-2 High Efficiency Video Coding Main/Main10/MSP(Main Still Picture) Profile
  - I/P slices
  - CTU64
    - Supported Prediction Unit(PU) size: 32x32, 16x16, 8x8
    - Supported Transform Unit(TU) size: 32x32 to 4x4
  - Parallel tools
    - Wavefront parallel processing (WPP) encoding with a single slice
    - Multi slice: Independent slice segment and dependent slice segment
  - High performance offline CABAC encoding
  - Motion estimation
    - 1/4-pel precision motion vectors
    - Search range [+/-128H, +/-64V] with an adaptive search center
    - Two reference frames for P-slice

  - Long-term reference for P picture and B picture
  - Custom tuning tools
  - Custom Lambda map and lambda table
  - Custom mode decision
  - Fully programmable user scaling list
- In-loop Filter
  - De-blocking filter
  - Sample adaptive offset (SAO)
  - Loop filtering across slices
- Weighted prediction
- Strong intra smoothing on/off
- Transform skip
- Lossless coding
- Picture/CTU/sub-CTU level of rate control
- Region of Interest (ROI) encoding with custom QP map
- Background encoding
- 3DNR

■ H.264/AVC Encoder

- Compatible with the ITU-T Recommendation H.264 specification. All coding tools in the profiles are supported
- With a few exceptions:
  - Interlaced coding tools are not supported
  - FMO/ASO tool of H.264 is not supported
- 16x16, 8x8 and 4x4 block sizes are supported and configurable
- Motion estimation
- 1/4-pel accuracy motion estimation with programmable search range up to [+/-64H, +/-32V]
- B picture with bi-prediction
- Two reference frames for P-slice
- Long-term reference for P picture and B picture
- Intra prediction
- Luma I4x4 Mode: 9 modes
- Luma I8x8 Mode: 9 modes
- Luma I16x16 Mode: 4 modes (Vertical, Horizon, DC, Plane)
- Chroma Mode: 3 modes (Vertical, Horizon, DC)
  - Custom tuning tools
  - User-defined mode (skip, intra) map
  - User-defined QP map

  - Lambda tuning for custom mode decision
  - Fully programmable user scaling list
- Weighted prediction (optional)
- In-loop de-blocking filter
- CABAC/CAVLC support
- Error resilience tools:
  - CIR (Cyclic Intra Refresh)
  - multi-slice structure
- A frame level and MB level of rate control
- Region of Interest (ROI) encoding with custom QP map

2.4.4 Video Decoder

- 4K 60frames X1 channel/sec or 1080p 30frames X8 channel/sec @ 450Mhz
- Support Format 420, 8-/10-bit
- Support I/P type slice
- HEVC Main/Main10, L5.1
- H.264 High/High10, L5.2
- 128bit AXI Bus interface
- Support Lossless Compression for frame buffer to save bandwidth
- Frame-based Processing promising the lowest burden to host processor for video operation
- Generating an interrupt when(ever) a specified number of MB-/CTU-rows are reached for low delay decoding
- H.264 decoding tools including:
  - Compatible with the ITU-T Recommendation H.264 specification
  - Support MVC Stereo High Profile
  - Support CABAC
  - Support CAVLC
  - Variable block size (16x16, 16x8, 8x16, 8x8, 4x8, and 4x4)
  - Interlaced coding tools are NOT supported
  - FMO/ASO is NOT supported
- HEVC decoding tools including:
  - Compatible with ISO/IEC 23008-2 High Efficiency Video Coding
  - I/P slices
    - All intra-prediction modes
    - All inter-prediction modes
  - Variable CTU size: 64x64 to 16x16

  - Variable Prediction Unit (PU) size: 64x64 to 4x4
  - Variable Transform Unit (TU) size: 32x32 to 4x4
- Advanced Motion Vector Prediction (AMVP) and merge mode
- ¼ Motion compensation with 8 tap filters
- Uniform reconstruction quantization (URQ)
- High performance CABAC decoding
- In-loop de-blocking filtering
- Sample Adaptive Offset (SAO)
- Loop filtering across slice/tile boundaries
- Data reporting to the external host
- Robust error concealment
- Sequence change detection

2.4.5 JPEG

- 290MPixel/sec for YUV420, 210MPixel/sec for YUV422, 140MPixel/sec for YUV444 @200Mhz
- Bit rate 480Mbps (MJPG 8M 30fps 422 1:8)
- Baseline/Extended sequential ISO/IEC 10918-1 JPEG compliance
- Compliant with Motion JPEG
- Support 1 or 3 color components
- 8-bit or 12-bit samples for each component - configurable
- Support 4:2:0, 4:2:2, 4:4:0, 4:4:4 and 4:0:0 color format (max. six 8x8 blocks in one MCU)
- Support from 16x16 pixels to 32K x 32K (32,768x32,768)
- Support ROI (Region of Interest) - decoder only
- Support 422/444 packed mode for all color formats
- After conversion to 422/444 color format
- Value-added features for encoding
  - Partial mode for encoding
  - On-the-fly rotator / mirror
- Value-added features for decoding
  - Partial mode for decoding
  - ROI (Region of Interest)
  - On-the-fly rotator / mirror
  - On-the-fly down sample

2.5 Display Subsystem

2.5.1 Display

- RGB656, RGB888 I/F, up to 1080p@60fps display
- Support 1/64-64 times scaler (1/64 not covered)
- Support MIPI TX DPHY lane connected with panel module

2.5.2 MIPI Display Interface

- MIPI TX DPHY
  - Support standard 8-bit/16-bit PPI interface compliant to MIPI D-PHY spec
  - Support 1 Clock Lane and up to 4 Data Lanes scalability
  - Support MIPI D-PHY HS-Tx data rate from 80Mbps up to 2.5Gbps. (< 0.1ppm/step)
  - Support MIPI D-PHY LP-Tx data rate of 10Mbps
  - Support Triggers, ULPS and LPDT
  - Support MIPI DSI and MIPI CSI applications.
  - Integrates switchable on-die termination
  - Support clock and data lane swapping function
  - Support reverse direction ULPS and LPDT

2.6 Connectivity Subsystem

2.6.1 USB 2.0/3.0

- USB2.0/3.0 controller
  - USB Interface:
    - Compliant with USB 3.0 Specification
    - Compliant with xHCI 1.0 Specification
    - SuperSpeed, Hi Speed and Full Speed supported
    - Single USB2.0 Port
    - Single USB3.0 Port
    - USB 3.0 PIPE interface compliant
    - USB 2.0 UTMI+ interface compliant
    - USB2 L1/L2 Support
    - USB3 U1/U2/U3 Support
  - Application Interface:
    - AXI3/4 Master Interface with 64-bit data and 32-bit address
    - APB4 Slave interface with 32-bit data and address
  - Dual Mode Operation:
    - HW selectable default mode selection supporting operation without any SW interaction

  - Programmable runtime mode change
  - Host Negotiate Protocol (HNP) support
  - SRP support
  - Separate Power Domains for Host and Peripheral Device logic
- Host Mode (CDNSXHCI):
  - Configurable total slots supported (maximum of 3264)
  - 32 endpoints per slot
  - 256 Primary Streams supported
  - MSI Support
  - Root Hub functionality implemented
  - xHCI Dynamic and Static Low Power Management Support
  - xHCI DMA engine with 64-bit @ 125MHz Full Duplex Data Path
- Peripheral Mode (USBSS-DEV):
  - Control transfers supported by Endpoint #0
  - Up to 15 IN and 15 OUT configurable/ programmable endpoints
  - Scatter-gather DMA
  - Dynamic data buffering
- Integrated Protocol Stack
  - Memory integration
  - Clock, reset and power management integration

- USB3.0 PHY
  - 5.0-Gbps super-speed data rate through 3m USB3.0 cable
  - Support 25MHz clock inputs
  - Support down-spread Spread Spectrum Clock (SSC) transmission and receiving (0~-5000ppm)
  - PIPE3.0 compliant interface for USB3.0
  - Support 16-bit interface at 250MHz operation and 32-bit interface at 125MHz operation
  - Support super-speed power down modes: U0, U1, U2 and U3
  - Integrated PHY with TX, RX, SSC, PLL, digital core and ESD
  - With adaptive RX equalizer to support different channel conditions
  - Accessible programmable controls allow user specific optimization of critical parameters
  - Integrated PLL to provide a variety of stand-alone clock outputs for USB related applications (25, 30, 48, 60, 120, 125 and 480MHz)
  - Provides robust BIST function for mass production tests
  - Built-in SSTX de-multiplexing and SSRX multiplexing for type-C or dual connectors
- USB2.0 PHY
  - 480-Mbps high-speed, 12-Mbps full-speed and 1.5-Mbps low-speed data transmission through 5m USB2.0 cable
  - Support USB2.0 normal mode, suspend, resume and remote wakeup

- Compliant with UTMI+ interface (High-speed, Full-speed, Low-speed and Preamble Packet)
- Support all USB2.0 test modes
- Built-in 45Ω termination and 1.5KΩ pull-up resistor
- SYNC and EOP generation and checking
- NRZI encoding and decoding
- Accessible register controls allow user specific optimization of critical parameters

2.6.2 Ethernet GMAC

- Compliant with IEEE 802.3 specifications
- Support for IEEE 1588-2002 and IEEE 1588-2008 standards including:
  - IEEE 802.3-az for Energy Efficient Ethernet (EEE)
  - IEEE 802.3x flow control automatic transmission of zero-quanta pause frame on flow control input de-assertion
  - IEEE 802.1Q VLAN tag detection for reception frames
- Support data transfer rates of 10/100/1000 Mbps
- Multiple TCP/IP offload functions supported
- Power Management Module (PMT) with remote wake-up frame and magic packet frame processing options
- RGMII, GMII, RMII, MII interface to communicate with an external gigabit PHY

2.6.3 CHIPLINK

- An off-chip serialization of the TileLink protocol, used to connect to an optional expansion board
- It is implemented as a source-synchronous single-data rate parallel bus
- Off-chip cache-coherent bus masters (e.g., in an FPGA)
- Off-chip memory-mapped slave devices
- Credit-based flow control to absorb off-chip latency
- Out-of-order completion to unblock concurrent operations
- Devices in the FPGA to connect their interrupts to the PLIC via this ChipLink bus

2.6.4 SD/SDIO/eMMC Host Controller

- 2 sets of Host Controller for SDIO devices
- 4-wire mode only
- Support up to 100MHz
- Support SD device of SD/mmc/SDIO WIFI module

2.7 Audio Interface

2.7.1 I2S

- Up to 4 set of I2S I/F (one for RX and three for TX)
- All I2S module support standard I2S format
- Support programmable sample rate: 16K/44.1K/48KHz
- Data resolution support up to 24bit (programmable support 16bit)
- Programmable FIFO depth up 32 for each channel
- All I2S module FIFO support DMA interface
- On-chip ADC or DAC can be bypassed with external codec device

2.7.2 S/PDIF

- 2 sets of S/PDIF, one for RX and one for TX mode
- Support sample rates from 44.1kHz up to 192kHz
- Support PCM format with a resolution of 16-bits or 24-bits per sample

2.7.3 PDM

- Support up to 4 channels with same sample rate
- Pulse Density Modulation interface for digital MIC interface
- Clock: 62.5K ~ 4MHz
- Down sampling to 24bit in SRC
- Combine clock source for each 2 channels
- I2S interface connect with I2S internally

2.7.4 PWMDAC

- The data format is 16bit, 8bit
- Support most sampling frequencies
- FIFO depth 8-byte
- Support two channels
- The resolution of PWM-DAC audio sampling supports 10bit and 8bit
- Data handling, software mode and DMA mode

2.8 Security Subsystem

2.8.1 Encryption Engines

- AES
- SHA
- ECC

- HASH

2.8.2 TRNG

- Compliant with NIST SP800-90a/b/c and BSI AIS 20/31
- Internal random seeding operation
- Host driven non-seeding option
- start-up continues and on-demand health test
- 128-bit random number generation
- 128 bits of security strength

2.8.3 OTP

- VDD and VDD2 Power Supply: 0.9V VDD, 1.8V VDD2 for Read and Program
- Memory Organization 512 x 32-bits (2KB)
- Bit Program Operation
- Data Retention: >10 Years
- Access Time: 50ns (max)
- Bit cell Program Time: 10us (min)

2.9 System Peripherals

2.9.1 SPI

- Up to 4 sets of SPI controller support Slave and Master mode, 1bit
- 1-wire data bit with speed up to 24M bps
- Support 8bit/16bit mode
- Separate data input and output bit
- Configurable FIFO size up to 8x16bit for both TX and RX channel
- Support DMA access for TX and RX FIFO

2.9.2 UART

- Up to 4 sets of UART controller
- 2 Support 2-wire mode
- 2 Support 4-wire mode (HW flow control with CTS/RTS)
- Separate up to 256Byte of TX and 384Byte of RX FIFOs
- Programmable FIFO disabling for 1-byte depth
- Programmable baud rate generator supports up to 3Mbps
- Support DMA access for TX and RX channel
- Standard asynchronous communication bits (start, stop and parity)

- Independent masking of transmit FIFO, receive FIFO, receive timeout, modem status, and error condition interrupts
- False start bit detection
- Line break generation and detection
- Programmable hardware flow control
- Fully-programmable serial interface characteristics
- Support 115200 baud rate

2.9.3 I2C

- 4 sets of I2C controller: 3 sets of master and 1 set of slaves
- Compatible with Philips I2C standard
- Support Multi Master Operation
- Software programmable clock frequency
- Clock Stretching and Wait state generation
- Software programmable acknowledge bit
- Interrupt or bit-polling driven byte-by-byte data-transfers
- Arbitration lost interrupt, with automatic transfer cancellation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection
- Bus busy detection
- Support 7 and 10bit addressing mode
- Operates from a wide range of input clock frequencies
- Support 100KHz/400KHz/1M mode

2.9.4 Timer

- 7 sets of 32-bit general purpose timer with individual maskable interrupts
- Register lock function
- Programmable output frequency

2.9.5 WDT

- 32 bits down counter
- Non-Maskable Interrupt (NMI) or WDOG reset
- Optional automatic WDOG reset if NMI handler fails to update the Watchdog register
- Maskable Watchdog freeze by user program
- Configurable clock source

2.9.6 Temp Sensor

- ±3°C untrimmed accuracy (-40ºC to 100ºC)

- ±1.0°C trimmed accuracy (0ºC to 70ºC)
- ±1.25°C trimmed accuracy (-40ºC to 125ºC)
- Calibration sequence requires no knowledge of die temperature
- Digital interface, 12bit resolution

2.9.7 PLL

- Dual power supply: 1.8V (analog)/0.9V(digital) allows for excellent supply noise rejection
- Output frequency range from 360MHz to 1.8GHz
- Duty cycle 50%±2%

2.9.8 INTC

- 2 INTC that support total 4 set of 32-bit source interrupt input
- Support separate interrupt with programmable type (level, edge) and polarity
- Software interrupt control

2.9.9 PWM

- 32-bit counter/timer facility
- single-run or continues run of PTC counter
- Programmable PWM mode
- System clock and external clock sources for timer functionality
- HI/LO Reference and Capture registers
- Three-state control for PWM output driver
- PWM/Timer/Counter functionalities can cause an interrupt to the CPU

2.9.10 Programmable Signals

- Overview

  There are two sets of programmable signal pins referred to as GPIOs and FUNC_SHAREs. A large number of signals, under the control of a programmable register, can be multiplexed on to these pins.

- GPIO
  - Support up to 64 GPIOs.
  - Programmable modes available to provide selected signals on these pins
  - Individually programmable input/output pins. Defaults to output at reset
  - Each GPIO has a dedicated control signal
  - Support separate interrupt with programmable type (level, edge) and polarity
  - All GPIO pins are also multiplexed on the functionally shared pins.
- Functionally Shared Pins (FUNC_SHAREs)
  - Support up to 142 functionally shared signal pins

- Programmable modes available to provide selected signals on these pins which includes proving the GPIO signals
- Individually programmable input/output pins, default to output at reset
- Each functionally shared pin has a dedicated control signal

3 Functional Block Diagram

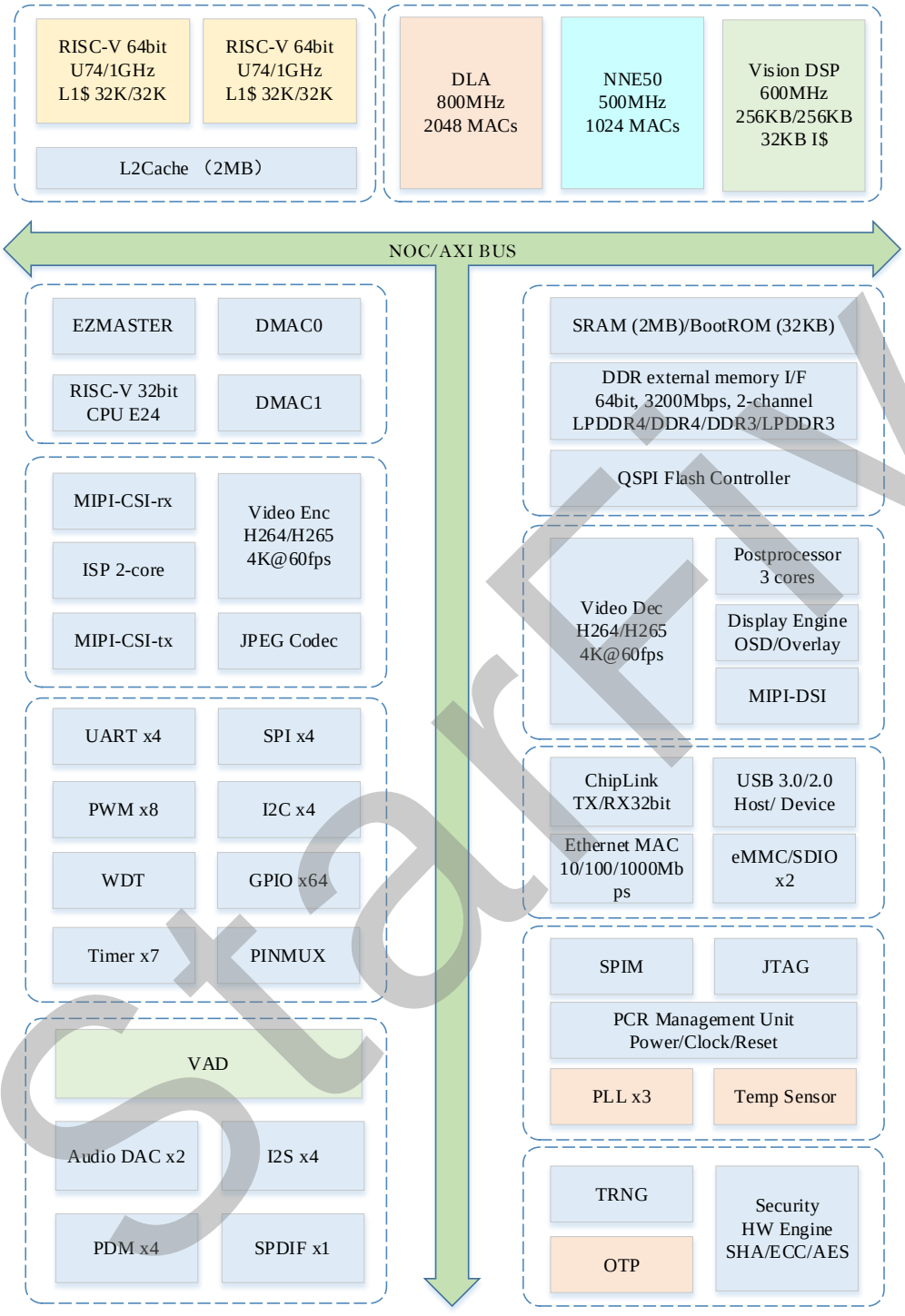


Figure 3-1 Function Block Diagram

4 Memory Map

Table 4-1 U74-MC Memory Map

Start Address	End Address	Size	Attribute	Usage	Notes
0x00_0000_0000	0x00_0000_0FFF		RWX A[1]	Debug	U74 Core
0x00_0000_1000	0x00_01FF_FFFF			Reserved	U74 Core
0x00_0200_0000	0x00_0200_FFFF		RW A	CLINT	U74 Core
0x00_0201_0000	0x00_0201_0FFF		RW A	Cache Controller	U74 Core
0x00_0201_1000	0x00_07FF_FFFF			Reserved	U74 Core
0x00_0800_0000	0x00_081F_FFFF		RWX A	L2 LIM	U74 Core
0x00_0820_0000	0x00_0BFF_FFFF			Reserved	U74 Core
0x00_0C00_0000	0x00_0FFF_FFFF		RW A	PLIC	U74 Core
0x00_1000_0000	0x00_17FF_FFFF	128MB	RW A	peripherals CSR	U74 Core
0x00_1800_0000	0x00_1FFF_FFFF	128MB	RWX	Internal RAM + ROM + slv	Internal ROM, Slave in system 0. 0x1800_0000 - 0x1801_FFFF, intRAM0 1. 0x1808_0000 - 0x1809_FFFF, intRAM1 2. 0x1840_0000 - 0x1840_7FFF, ROM 3. 0x1900_0000 - 0x193F_FFFF, reserved 4. 0x1940_0000 - 0x195F_FFFF, reserved

[1] Memory attributes: **R** - Read, **W** -Write, **X** - Execute, **C** - Cacheable, **A** - Atomics

Start Address	End Address	Size	Attribute	Usage	Notes
					5. 0x1960_0000 - 0x197F_FFFF, NNE slave 6. 0x1980_0000 - 0x19BF_FFFF, ISP slave 7. 0x19C0_0000 - 0x19FF_FFFF, DLA slave
0x00_2000_0000	0x00_3FFF_FFFF	256MB	RWX	QSPI	off-chip QSPI NOR/NAND flash, belong to JH7100
0x00_4000_0000	0x00_40FF_FFFF	16MB	RWX	VP6 slv	
0x00_4100_0000	0x00_5FFF_FFFF	496MB	RWX	ChipLink	Non-cacheable space. Remapped to 0x00_6100_0000 - 0x00_7FFF_FFFF
0x10_0000_0000	0x17_FFFF_FFFF	32GB	RWX	DDR	Off-chip DDR, belong to JH7100, non-cacheable. remapped to 0x00_8000_0000 - 0x08_7FFF_FFFF
0x20_0000_0000	0x2F_FFFF_FFFF	64GB	RWX	ChipLink	ChipLink, non-cacheable space, remapped to 0x30_0000_0000 - 0x3F_FFFF_FFFF
0x00_6100_0000	0x00_7FFF_FFFF	496MB	RWX C A	ChipLink	ChipLink, cacheable, the same physical memory with system port 0x00_4000_0000 - 0x00_5000_0000 space
0x00_8000_0000	0x08_7FFF_FFFF	32GB	RWX C A	DDR	Off-chip DDR, belong to JH7100, the same physical memory with system port 0x00_8000_0000 - 0x08_7000_0000 space
0x30_0000_0000	0x3F_FFFF_FFFF	64GB	RWX C A	ChipLink	ChipLink, cacheable, the same physical memory with system port 0x20_0000_0000 - 0x2F_0000_0000 space

Table 4-2 Peripherals Port Memory Map

Peripherals Port	Start Address	End Address	Size
SDIO0_CSR	0x00_1000_0000	0x00_1000_FFFF	64KB
SDIO1_CSR	0x00_1001_0000	0x00_1001_FFFF	64KB
GMAC_CSR	0x00_1002_0000	0x00_1002_FFFF	64KB
EZMASTER_CSR	0x00_1003_0000	0x00_100A_FFFF	512KB
SGDMA2P_CSR	0x00_100B_0000	0x00_100B_FFFF	64KB
RESERVED	0x00_100C_0000	0x00_100C_FFFF	
SECENGINE	0x00_100D_0000	0x00_100E_FFFF	128KB
SPI2AHB_CSR	0x00_100F_0000	0x00_100F_FFFF	64KB
GPU2D_CSR	0x00_1010_0000	0x00_1013_FFFF	256KB
RESERVED	0x00_1014_0000	0x00_103F_FFFF	
I2SADC	0x00_1040_0000	0x00_1040_FFFF	64KB
PDM	0x00_1041_0000	0x00_1041_FFFF	64KB
VAD	0x00_1042_0000	0x00_1042_FFFF	64KB
SPDIF	0x00_1043_0000	0x00_1043_FFFF	64KB
PWMDAC	0x00_1044_0000	0x00_1044_FFFF	64KB
I2SDAC0	0x00_1045_0000	0x00_1045_FFFF	64KB
I2SDAC1	0x00_1046_0000	0x00_1046_FFFF	64KB
I2SDAC16K	0x00_1047_0000	0x00_1047_FFFF	64KB
DOM_AUDIO_CLKGEN	0x00_1048_0000	0x00_1048_FFFF	64KB
DOM_AUDIO_RSTGEN	0x00_1049_0000	0x00_1049_FFFF	64KB
DOM_AUDIO_SYSCTRL	0x00_104A_0000	0x00_104A_FFFF	64KB
USB	0x00_104C_0000	0x00_104F_FFFF	256KB
SGDMA1P	0x00_1050_0000	0x00_1050_FFFF	64KB
NNE_CSR	0x00_1080_0000	0x00_108F_FFFF	1MB
RESERVED	0x00_1090_0000	0x00_10FF_FFFF	4MB
NOC_CSR	0x00_1100_0000	0x00_117F_FFFF	8MB
CLKGEN_CSR	0x00_1180_0000	0x00_1180_FFFF	64KB
OTP	0x00_1181_0000	0x00_1181_FFFF	64KB
DDRPHY0_CSR	0x00_1182_0000	0x00_1182_FFFF	64KB
DDRPHY1_CSR	0x00_1183_0000	0x00_1183_FFFF	64KB

Peripherals Port	Start Address	End Address	Size
RSTGEN_CSR	0x00_1184_0000	0x00_1184_FFFF	64KB
SYSCTRL-MAINSYS	0x00_1185_0000	0x00_1185_3FFF	16KB
SYSCTRL-REMAP_VP6NOC	0x00_1185_4000	0x00_1185_7FFF	16KB
SYSCTRL-IOPAD_CTRL	0x00_1185_8000	0x00_1185_BFFF	16KB
SYSCTRL_SIMU_TEST	0x00_1185_C000	0x00_1185_FFFF	16KB
QSPI_CSR	0x00_1186_0000	0x00_1186_FFFF	64KB
HSUART0	0x00_1187_0000	0x00_1187_FFFF	64KB
HSUART1	0x00_1188_0000	0x00_1188_FFFF	64KB
SPI0	0x00_1189_0000	0x00_1189_FFFF	64KB
SPI1	0x00_118A_0000	0x00_118A_FFFF	64KB
I2C0	0x00_118B_0000	0x00_118B_FFFF	64KB
I2C1	0x00_118C_0000	0x00_118C_FFFF	64KB
TRNG	0x00_118D_0000	0x00_118D_FFFF	64KB
VENC_CSR	0x00_118E_0000	0x00_118E_EFFF	64KB
VDEC_CSR	0x00_118F_0000	0x00_118F_EFFF	64KB
JPEG_CSR	0x00_1190_0000	0x00_1190_FFFF	64KB
GPIO	0x00_1191_0000	0x00_1191_FFFF	64KB
DLA_CSR	0x00_1194_0000	0x00_1197_FFFF	256KB
VP6_APB	0x00_11A0_0000	0x00_11AF_FFFF	1MB
RESERVED	0x00_11B0_0000	0x00_11FF_FFFF	
LCDC	0x00_1200_0000	0x00_1200_FFFF	64KB
VPP0	0x00_1204_0000	0x00_1204_FFFF	64KB
VPP1	0x00_1208_0000	0x00_1208_FFFF	64KB
DSITX	0x00_1210_0000	0x00_1210_FFFF	64KB
VPP2	0x00_120c_0000	0x00_120c_FFFF	64KB
PIXRAWOUT	0x00_1220_0000	0x00_1220_FFFF	64KB
MAP_CONVERTER	0x00_1221_0000	0x00_1221_FFFF	64KB
CSI2TX	0x00_1222_0000	0x00_1222_FFFF	64KB
VOUT_CLKGEN	0x00_1224_0000	0x00_1224_FFFF	64KB
VOUT_RSTGEN	0x00_1225_0000	0x00_1225_FFFF	64KB
VOUT_SYSCON	0x00_1226_0000	0x00_1226_FFFF	64KB

Peripherals Port	Start Address	End Address	Size
VP6_INTC0	0x00_1240_0000	0x00_1240_FFFF	64KB
SPI2	0x00_1241_0000	0x00_1241_FFFF	64KB
SPI3	0x00_1242_0000	0x00_1242_FFFF	64KB
UART2	0x00_1243_0000	0x00_1243_FFFF	64KB
UART3	0x00_1244_0000	0x00_1244_FFFF	64KB
I2C2	0x00_1245_0000	0x00_1245_FFFF	64KB
I2C3	0x00_1246_0000	0x00_1246_FFFF	64KB
CHIPLINK/MSI SLAVE	0x00_1247_0000	0x00_1247_7FFF	32KB
CHIPLINK/ERROR_DEVICE	0x00_1247_8000	0x00_1247_FFFF	32KB
WDT	0x00_1248_0000	0x00_1248_FFFF	64KB
PWM	0x00_1249_0000	0x00_1249_FFFF	64KB
TEMPSENSOR	0x00_124A_0000	0x00_124A_FFFF	64KB
VP6_INTC1	0x00_124B_0000	0x00_124B_FFFF	64KB
SYS_ERRDEV_CSR	0x00_124C_0000	0x00_124C_FFFF	64KB
RESERVED (ILLEGAL)	0x00_124D_0000	0x00_17FF_FFFF	

5 System Application Diagram

The following figure shows the full feature application for JH7100:

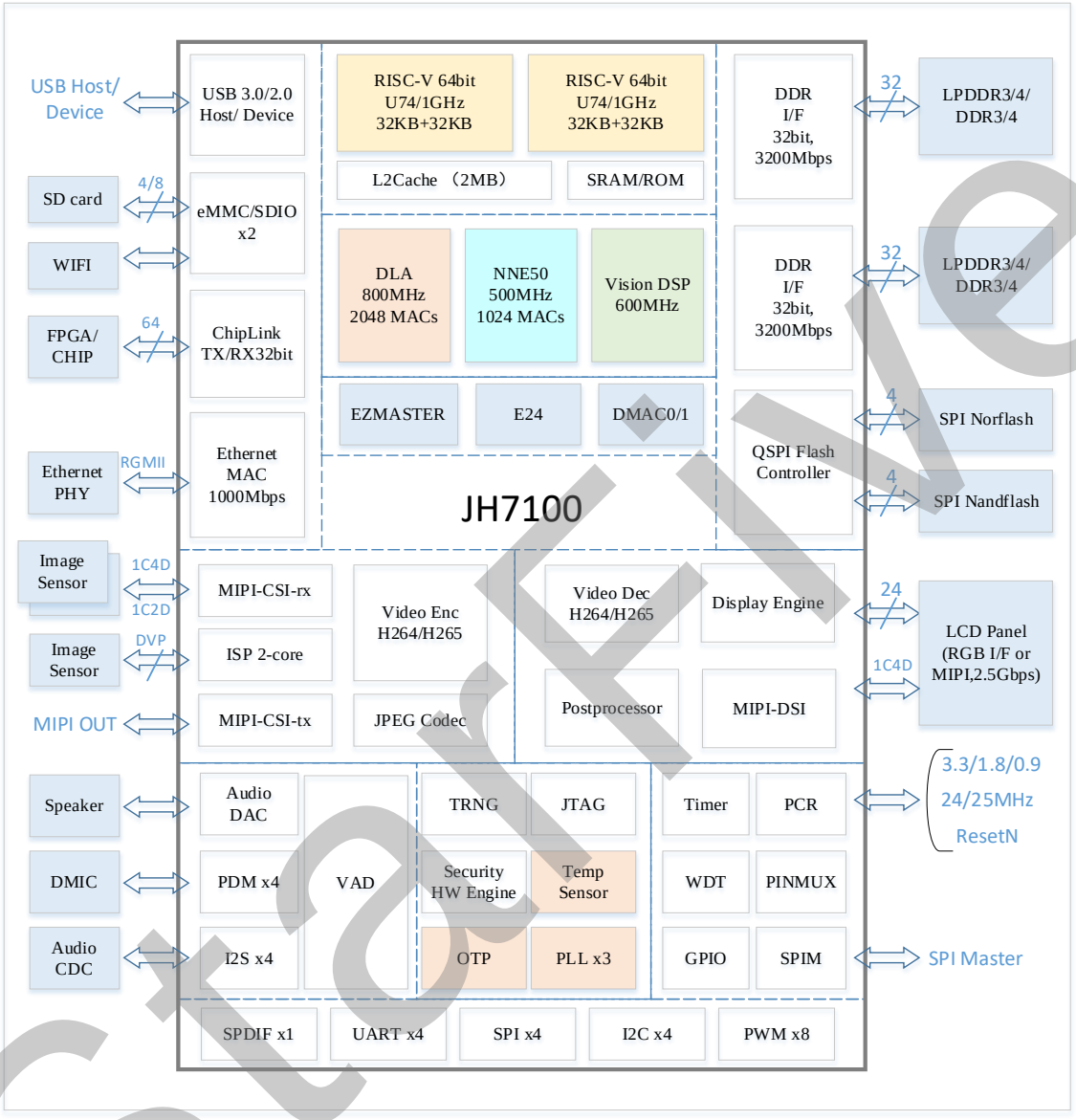


Figure 5-1 Full Feature Application

Diagrams for the following applications are:

- AI Enabled Multimedia AP
- Smart Camera Application
- Smart AV Application

6 System Boot Method and Sequence

For detailed boot flow, the boot sources available for the JH7100 SoC and the bare metal boot examples, refer to *JH7100 SoC Boot User Guide*.

7 Clock & Reset

7.1 Clock Source

- Two external oscillator OSC0 and OSC1 input
  - OSC0 25M default for USB, GMAC and system main clock source
  - OSC1 input 12-27MHz according to application
- Three PLLs
  - PLL0 used for system main logic, including CPU, bus
  - PLL1 output to support DDR, DLA and DSP
  - PLL2 output to support slow speed peripherals, video input and video output

7.2 Reset

pad_rstn is an asynchronous active low reset that can be connected to an external reset device output. There is not internal de-bounce logic.

rst_pll, *rstn_clkgen*, and *rstn_sys* are generated by internal synchronous resets for respective clock domains.

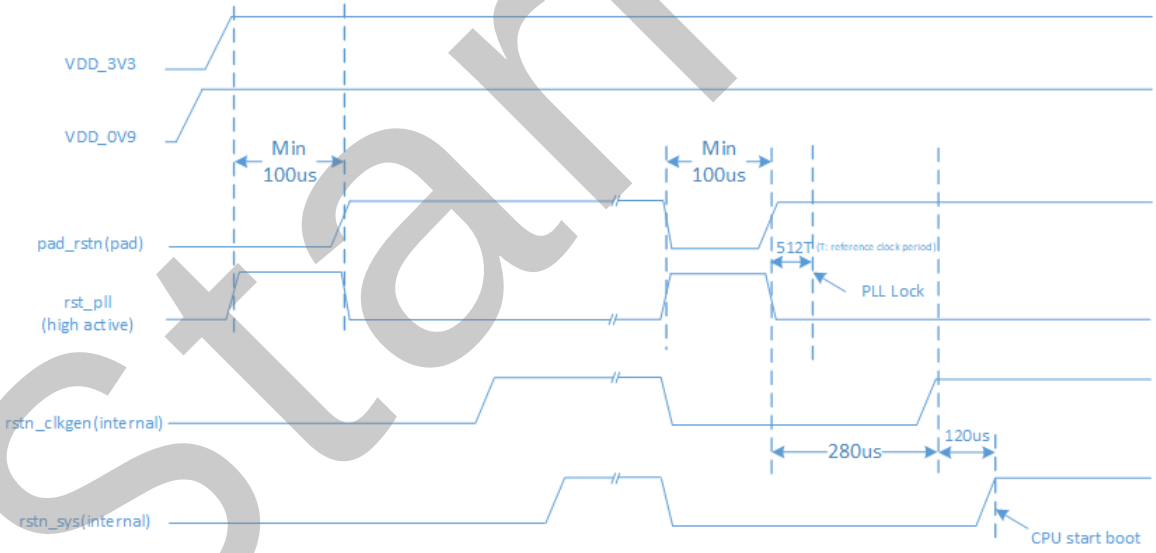


Figure 7-1 Reset timing

8 Chip Power On/Off Sequence

- Power-up/down sequence
  - No limitation for core VDD power-up/down sequence: VDD can be powered on/off first or last.
- Power-up
  - First power up 1.8V by external 1.8V system power through PVDD18RGM; after at least 20us, power up 3.3V through PVDD3RGM.
- Power-down
  - First power down 3.3V through PVDD3RGM; after at least 20us, power down 1.8V system power through PVDD18RGM.

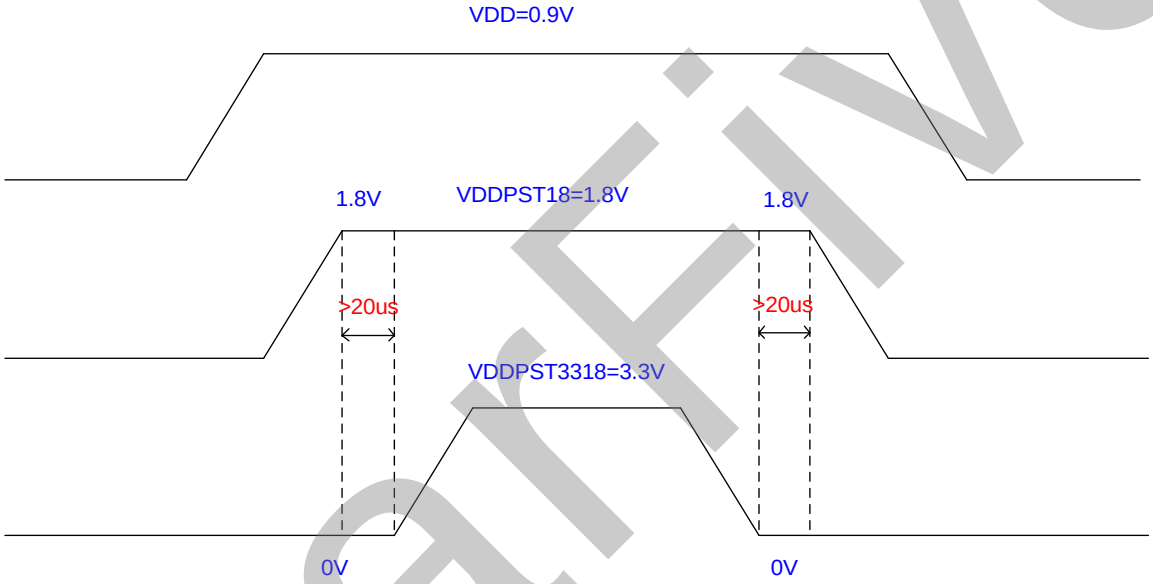


Figure 8-1 Chip Power on/off Sequence

9 Pin List and Ball map

9.1 Pin List & Description

Table 9-1 Pin List

Pin Number	Pin Name	IO-Type	Description
A1	DDR0_DQ[30]	DDR	DDR SDRAM0 data [30]
A2	DDR0_DQ[24]	DDR	DDR SDRAM0 data [24]
A3	DDR0_DQ[26]	DDR	DDR SDRAM0 data [26]
A4	VSS	VSS	digital ground
A5	DDR0_DQ[16]	DDR	DDR SDRAM0 data [16]
A6	DDR0_DQS_P[2]	DDR	DDR SDRAM0 Data Strobe DQS2_P
A7	VSS	VSS	digital ground
A9	DDR0_ACT_N	DDR	DDR SDRAM0 ACT_n
A10	DDR0_ADR[11]	DDR	DDR SDRAM0 Address [11]
A11	VSS	VSS	digital ground
A12	DDR0_CK_P[1]	DDR	DDR SDRAM0 differential clock inputs CK1_P
A14	DDR0_CK_P[0]	DDR	DDR SDRAM0 differential clock inputs CK0_P
A15	DDR0_ADR[2]	DDR	DDR SDRAM0 Address [2]
A16	DDR0_ATB0	DDR	DDR0 PHY IO pad Analog Test Bus (ATB)
A17	DDR0_CS_N[1]	DDR	DDR SDRAM0 CS1
A18	VSS	VSS	digital ground
A19	DDR0_DQ[15]	DDR	DDR SDRAM0 data [15]
A20	DDR0_DQS_N[1]	DDR	DDR SDRAM0 Data Strobe DQS1_N
A21	DDR0_DQ[8]	DDR	DDR SDRAM0 data [8]
A22	DDR0_DQ[7]	DDR	DDR SDRAM0 data [7]
A23	DDR0_DQ[6]	DDR	DDR SDRAM0 data [6]
A25	GPIO[0]	IO	function IO share with GPIO
A26	GPIO[3]	IO	function IO share with GPIO
A27	GPIO[6]	IO	function IO share with GPIO
A28	GPIO[9]	IO	function IO share with GPIO

Pin Number	Pin Name	IO-Type	Description
A29	GPIO[12]	IO	function IO share with GPIO
A30	GPIO[15]	IO	function IO share with GPIO
A31	GPIO[17]	IO	function IO share with GPIO
AA1	FUNC_SHARE[72]	IO	function IO share with group
AA2	FUNC_SHARE[77]	IO	function IO share with group
AA3	FUNC_SHARE[70]	IO	function IO share with group
AA4	FUNC_SHARE[71]	IO	function IO share with group
AA5	FUNC_SHARE[74]	IO	function IO share with group
AA6	FUNC_SHARE[75]	IO	function IO share with group
AA8	VSS	VSS	digital ground
AA9	VDD3318_SENSOR	VDD3318	FUNC_SHARE[98-114] IO power
AA10	VSS	VSS	digital ground
AA11	VDD	VDD	digital core power
AA12	VSS	VSS	digital ground
AA13	VSS	VSS	digital ground
AA14	VSS	VSS	digital ground
AA15	VSS	VSS	digital ground
AA16	VDDQCK_DDR1	DDR	DDR CK power
AA17	VSS	VSS	digital ground
AA18	VDDPLL_DDR1	DDR	DDR PLL power
AA19	VSS	VSS	digital ground
AA20	VSS	VSS	digital ground
AA21	VDD3318_GMII	VDD3318	FUNC_SHARE[115-141] IO power
AA22	VSS	VSS	digital ground
AA23	AVDD33_USB	AVDD33	USB analog power supply
AA24	AVSS_USB	AVSS	USB analog ground
AA25	FUNC_SHARE[121]	IO	function IO share with group
AA26	FUNC_SHARE[120]	IO	function IO share with group
AA27	FUNC_SHARE[115]	IO	function IO share with group
AA28	FUNC_SHARE[124]	IO	function IO share with group
AA29	VSS	VSS	digital ground

Pin Number	Pin Name	IO-Type	Description
AA30	FUNC_SHARE[125]	IO	function IO share with group
AA31	FUNC_SHARE[128]	IO	function IO share with group
AB1	FUNC_SHARE[76]	IO	function IO share with group
AB2	FUNC_SHARE[81]	IO	function IO share with group
AB3	VSS	VSS	digital ground
AB4	FUNC_SHARE[85]	IO	function IO share with group
AB5	FUNC_SHARE[78]	IO	function IO share with group
AB6	FUNC_SHARE[79]	IO	function IO share with group
AB7	FUNC_SHARE[82]	IO	function IO share with group
AB8	VSS	VSS	digital ground
AB9	VDD3318_SENSOR	VDD3318	FUNC_SHARE[98-114] IO power
AB10	VSS	VSS	digital ground
AB11	VSS	VSS	digital ground
AB12	VDDQ_DDR1	DDR	DDR IO power
AB13	VDDQ_DDR1	DDR	DDR IO power
AB14	VDDQ_DDR1	DDR	DDR IO power
AB15	VDDQ_DDR1	DDR	DDR IO power
AB16	VDDQ_DDR1	DDR	DDR IO power
AB17	VSS	VSS	digital ground
AB18	VDDQ_DDR1	DDR	DDR IO power
AB19	VSS	VSS	digital ground
AB20	VSS	VSS	digital ground
AB21	DVDD18_OTP	DVDD18	OTP power
AB22	VSS18_OTP	VSS	OTP ground
AB30	FUNC_SHARE[117]	IO	function IO share with group
AB31	FUNC_SHARE[119]	IO	function IO share with group
AC1	FUNC_SHARE[80]	IO	function IO share with group
AC8	VSS	VSS	digital ground
AC9	VSS	VSS	digital ground
AC10	VSS	VSS	digital ground
AC11	VDDQ_DDR1	DDR	DDR IO power

Pin Number	Pin Name	IO-Type	Description
AC12	VDDQ_DDR1	DDR	DDR IO power
AC13	VDDQ_DDR1	DDR	DDR IO power
AC14	VSS	VSS	digital ground
AC15	VSS	VSS	digital ground
AC16	VDDQ_DDR1	DDR	DDR IO power
AC17	VSS	VSS	digital ground
AC18	VDDQ_DDR1	DDR	DDR IO power
AC19	VSS	VSS	digital ground
AC20	VSS	VSS	digital ground
AC21	ANA18_OTP_PENVDD2	ANA18	OTP VDD2 power enable flag
AC22	VSS	VSS	digital ground
AC23	AVDD09TX_USB	AVDD	USB TX analog power
AC24	AVSSTX_USB	AVSS	USB TX analog ground
AC25	VSS	VSS	digital ground
AC26	USB_SSTXB1	USB	USB 3.0 TX P signal
AC27	USB_SSTXA1	USB	USB 3.0 TX P signal
AC28	USB_DP	USB	USB 2.0 DP
AC29	USB_DM	USB	USB 2.0 DM
AC30	USB_SSRXB2	USB	USB 3.0 RX M signal
AC31	USB_SSRXA2	USB	USB 3.0 RX P signal
AD1	FUNC_SHARE[84]	IO	function IO share with group
AD2	FUNC_SHARE[89]	IO	function IO share with group
AD3	FUNC_SHARE[92]	IO	function IO share with group
AD4	FUNC_SHARE[96]	IO	function IO share with group
AD5	FUNC_SHARE[97]	IO	function IO share with group
AD6	FUNC_SHARE[102]	IO	function IO share with group
AD7	FUNC_SHARE[101]	IO	function IO share with group
AD8	VDDQ_DDR1	DDR	DDR IO power
AD9	VDDQ_DDR1	DDR	DDR IO power
AD10	VDDQ_DDR1	DDR	DDR IO power
AD11	VDDQ_DDR1	DDR	DDR IO power

Pin Number	Pin Name	IO-Type	Description
AD12	VDDQ_DDR1	DDR	DDR IO power
AD13	VSS	VSS	digital ground
AD14	VSS	VSS	digital ground
AD15	VSS	VSS	digital ground
AD16	VDDQ_DDR1	DDR	DDR IO power
AD17	VDDQ_DDR1	DDR	DDR IO power
AD18	VDDQ_DDR1	DDR	DDR IO power
AD19	VSS	VSS	digital ground
AD20	VSS	VSS	digital ground
AD21	VSS	VSS	digital ground
AD22	VSS	VSS	digital ground
AD23	AVDD09RX_USB	AVDD	USB RX analog power
AD24	AVDD18_USB	AVDD18	USB analog power
AD25	VSS	VSS	digital ground
AD26	USB_SSRXB1	USB	USB 3.0 RX M signal
AD27	USB_SSRXA1	USB	USB 3.0 RX P signal
AD28	VSS	VSS	digital ground
AD29	VSS	VSS	digital ground
AD30	USB_SSTXA2	USB	USB 3.0 TX P signal
AD31	USB_SSTXB2	USB	USB 3.0 TX P signal
AE1	FUNC_SHARE[88]	IO	function IO share with group
AE2	FUNC_SHARE[93]	IO	function IO share with group
AE3	VSS	VSS	digital ground
AE4	FUNC_SHARE[94]	IO	function IO share with group
AE5	FUNC_SHARE[104]	IO	function IO share with group
AE6	FUNC_SHARE[108]	IO	function IO share with group
AE7	FUNC_SHARE[112]	IO	function IO share with group
AE8	VSS	VSS	digital ground
AE9	VDDQ_DDR1	DDR	DDR IO power
AE10	VDDQ_DDR1	DDR	DDR IO power
AE11	VSS	VSS	digital ground

Pin Number	Pin Name	IO-Type	Description
AE12	VDDQ_DDR1	DDR	DDR IO power
AE13	DDR1_ADR[9]	DDR	DDR SDRAM1 Address [9]
AE14	VSS	VSS	digital ground
AE15	VSS	VSS	digital ground
AE16	DDR1_BG[0]	DDR	DDR SDRAM1 Bank Group0
AE17	VDDQ_DDR1	DDR	DDR IO power
AE18	DDR1_CAS_N_ADR15	DDR	DDR SDRAM1 Address 15
AE19	VDDQ_DDR1	DDR	DDR IO power
AE20	VSS	VSS	digital ground
AE21	VDDQ_DDR1	DDR	DDR IO power
AE22	VDDQ_DDR1	DDR	DDR IO power
AE23	AVSSRX_USB	AVSS	USB RX analog ground
AE24	VSS	VSS	digital ground
AE31	VSS	VSS	digital ground
AF1	FUNC_SHARE[99]	IO	function IO share with group
AF7	DDR1_DQ[31]	DDR	DDR SDRAM1 data [31]
AF8	DDR1_DQ[28]	DDR	DDR SDRAM1 data [28]
AF10	DDR1_DQ[23]	DDR	DDR SDRAM1 data [23]
AF11	DDR1_DQ[22]	DDR	DDR SDRAM1 data [22]
AF13	DDR1_ADR[6]	DDR	DDR SDRAM1 Address [6]
AF14	DDR1_ADR[3]	DDR	DDR SDRAM1 Address [3]
AF16	DDR1_BA[1]	DDR	DDR SDRAM1 Bank Address 1
AF18	DDR1_WE_N_ADR14	DDR	DDR SDRAM1 Address 14
AF20	DDR1_CS_N[3]	DDR	DDR SDRAM1 CS3
AF21	DDR1_PLL_REFOUT_N	DDR	DDR1 PHY Differential PLL reference clock output
AF23	DDR1_DQ[15]	DDR	DDR SDRAM1 data [15]
AF24	DDR1_DQ[14]	DDR	DDR SDRAM1 data [14]
AF26	DDR1_DQ[8]	DDR	DDR SDRAM1 data [8]
AF27	VSS	VSS	digital ground
AF29	DDR1_DQ[0]	DDR	DDR SDRAM1 data [0]
AF30	DDR1_DQ[3]	DDR	DDR SDRAM1 data [3]

Pin Number	Pin Name	IO-Type	Description
AG1	FUNC_SHARE[100]	IO	function IO share with group
AG2	FUNC_SHARE[83]	IO	function IO share with group
AG3	FUNC_SHARE[87]	IO	function IO share with group
AG4	FUNC_SHARE[91]	IO	function IO share with group
AG5	VSS	VSS	digital ground
AG7	DDR1_DQ[30]	DDR	DDR SDRAM1 data [30]
AG8	DDR1_DQ[29]	DDR	DDR SDRAM1 data [29]
AG10	DDR1_DQ[20]	DDR	DDR SDRAM1 data [20]
AG11	DDR1_DM_DBI_N[2]	DDR	DDR SDRAM1 Input Data Mask and Data Bus Inversion for byte0
AG14	DDR1_ADR[5]	DDR	DDR SDRAM1 Address [5]
AG16	DDR1_ADR[0]	DDR	DDR SDRAM1 Address [0]
AG18	VSS	VSS	digital ground
AG20	DDR1_CAL	DDR	DDR1 PHY IO pad calibration resistor connection
AG21	DDR1_PLL_REFOUT_P	DDR	DDR1 PHY Differential PLL reference clock output
AG23	DDR1_CKE[0]	DDR	DDR SDRAM1 Clock0 enable
AG24	VSS	VSS	digital ground
AG26	DDR1_DQ[11]	DDR	DDR SDRAM1 data [11]
AG27	DDR1_DQ[10]	DDR	DDR SDRAM1 data [10]
AG29	DDR1_DQ[1]	DDR	DDR SDRAM1 data [1]
AG30	DDR1_DM_DBI_N[0]	DDR	DDR SDRAM1 Input Data Mask and Data Bus Inversion for byte0
AH1	FUNC_SHARE[103]	IO	function IO share with group
AH2	FUNC_SHARE[86]	IO	function IO share with group
AH3	VSS	VSS	digital ground
AH4	FUNC_SHARE[95]	IO	function IO share with group
AH5	FUNC_SHARE[106]	IO	function IO share with group
AH7	VSS	VSS	digital ground
AH8	DDR1_DM_DBI_N[3]	DDR	DDR SDRAM1 Input Data Mask and Data Bus Inversion for byte0
AH10	VSS	VSS	digital ground
AH11	DDR1_DQ[21]	DDR	DDR SDRAM1 data [21]

Pin Number	Pin Name	IO-Type	Description
AH13	VSS	VSS	digital ground
AH14	DDR1_ADR[7]	DDR	DDR SDRAM1 Address [7]
AH16	VSS	VSS	digital ground
AH18	DDR1_PAR	DDR	DDR SDRAM1 PAR0
AH20	DDR1_CS_N[2]	DDR	DDR SDRAM1 CS2
AH21	DDR1_CS_N[1]	DDR	DDR SDRAM1 CS1
AH23	DDR1_ODT[1]	DDR	DDR SDRAM1 On Die Termination for CS1
AH24	DDR1_ODT[0]	DDR	DDR SDRAM1 On Die Termination for CS0
AH26	VSS	VSS	digital ground
AH27	DDR1_DQ[9]	DDR	DDR SDRAM1 data [9]
AH29	VSS	VSS	digital ground
AH30	DDR1_DQ[2]	DDR	DDR SDRAM1 data [2]
AJ1	FUNC_SHARE[105]	IO	function IO share with group
AJ7	DDR1_DQS_P[3]	DDR	DDR SDRAM1 Data Strobe DQS3_P
AJ8	DDR1_DQ[27]	DDR	DDR SDRAM1 data [27]
AJ10	DDR1_DQS_N[2]	DDR	DDR SDRAM1 Data Strobe DQS2_N
AJ11	DDR1_DQ[19]	DDR	DDR SDRAM1 data [19]
AJ12	DDR1_BG[1]	DDR	DDR SDRAM1 Bank Group1
AJ13	DDR1_ADR[12]	DDR	DDR SDRAM1 Address [12]
AJ14	DDR1_ADR[10]	DDR	DDR SDRAM1 Address [10]
AJ16	DDR1_ADR[2]	DDR	DDR SDRAM1 Address [2]
AJ18	DDR1_ADR[1]	DDR	DDR SDRAM1 Address [1]
AJ20	DDR1_ERR_N	DDR	DDR SDRAM1 alert_n
AJ21	VSS	VSS	digital ground
AJ23	VSS	VSS	digital ground
AJ24	DDR1_CKE[1]	DDR	DDR SDRAM1 Clock1 enable
AJ26	DDR1_DM_DBI_N[1]	DDR	DDR SDRAM1 Input Data Mask and Data Bus Inversion for byte0
AJ27	DDR1_DQS_P[1]	DDR	DDR SDRAM1 Data Strobe DQS1_P
AJ29	DDR1_DQ[4]	DDR	DDR SDRAM1 data [4]
AJ30	DDR1_DQS_N[0]	DDR	DDR SDRAM1 Data Strobe DQS0_N

Pin Number	Pin Name	IO-Type	Description
AK1	FUNC_SHARE[107]	IO	function IO share with group
AK2	FUNC_SHARE[109]	IO	function IO share with group
AK3	VSS	VSS	digital ground
AK4	FUNC_SHARE[98]	IO	function IO share with group
AK5	VSS	VSS	digital ground
AK7	DDR1_DQS_N[3]	DDR	DDR SDRAM1 Data Strobe DQS3_N
AK8	DDR1_DQ[26]	DDR	DDR SDRAM1 data [26]
AK10	DDR1_DQS_P[2]	DDR	DDR SDRAM1 Data Strobe DQS2_P
AK11	DDR1_DQ[17]	DDR	DDR SDRAM1 data [17]
AK12	DDR1_ADR[13]	DDR	DDR SDRAM1 Address [13]
AK13	DDR1_ACT_N	DDR	DDR SDRAM1 ACT_n
AK14	DDR1_ADR[8]	DDR	DDR SDRAM1 Address [8]
AK16	DDR1_CK_N[1]	DDR	DDR SDRAM1 differential clock inputs CK1_N
AK18	DDR1_CK_N[0]	DDR	DDR SDRAM1 differential clock inputs CK0_N
AK20	DDR1_RAS_N_ADR16	DDR	DDR SDRAM1 Address 16
AK21	DDR1_ATB0	DDR	DDR1 PHY IO pad Analog Test Bus (ATB)
AK23	DDR1_CS_N[0]	DDR	DDR SDRAM1 CS0
AK24	DDR1_PLL_TESTOUT_N	DDR	DDR1 PHY Differential PLL test clock output
AK26	VSS	VSS	digital ground
AK27	DDR1_DQS_N[1]	DDR	DDR SDRAM1 Data Strobe DQS1_N
AK29	DDR1_DQ[5]	DDR	DDR SDRAM1 data [5]
AK30	DDR1_DQS_P[0]	DDR	DDR SDRAM1 Data Strobe DQS0_P
AL1	FUNC_SHARE[111]	IO	function IO share with group
AL2	FUNC_SHARE[113]	IO	function IO share with group
AL3	FUNC_SHARE[90]	IO	function IO share with group
AL4	FUNC_SHARE[110]	IO	function IO share with group
AL5	FUNC_SHARE[114]	IO	function IO share with group
AL6	VSS	VSS	digital ground
AL7	DDR1_DQ[25]	DDR	DDR SDRAM1 data [25]
AL8	DDR1_DQ[24]	DDR	DDR SDRAM1 data [24]
AL9	VSS	VSS	digital ground

Pin Number	Pin Name	IO-Type	Description
AL10	DDR1_DQ[18]	DDR	DDR SDRAM1 data [18]
AL11	DDR1_DQ[16]	DDR	DDR SDRAM1 data [16]
AL12	VSS	VSS	digital ground
AL13	DDR1_ADR[11]	DDR	DDR SDRAM1 Address [11]
AL14	DDR1_ADR[4]	DDR	DDR SDRAM1 Address [4]
AL15	VSS	VSS	digital ground
AL16	DDR1_CK_P[1]	DDR	DDR SDRAM1 differential clock inputs CK1_P
AL18	DDR1_CK_P[0]	DDR	DDR SDRAM1 differential clock inputs CK0_P
AL19	VSS	VSS	digital ground
AL20	DDR1_BA[0]	DDR	DDR SDRAM1 Bank Address 0
AL21	DDR1_ATB1	DDR	DDR1 PHY IO pad Analog Test Bus (ATB)
AL22	VSS	VSS	digital ground
AL23	DDR1_RESET_N	DDR	DDR SDRAM1 Active Low Asynchronous Reset
AL24	DDR1_PLL_TESTOUT_P	DDR	DDR1 PHY Differential PLL test clock output
AL25	VSS	VSS	digital ground
AL26	DDR1_DQ[13]	DDR	DDR SDRAM1 data [13]
AL27	DDR1_DQ[12]	DDR	DDR SDRAM1 data [12]
AL28	VSS	VSS	digital ground
AL29	DDR1_DQ[7]	DDR	DDR SDRAM1 data [7]
AL30	DDR1_DQ[6]	DDR	DDR SDRAM1 data [6]
B1	DDR0_DQ[29]	DDR	DDR SDRAM0 data [29]
B2	DDR0_DQ[28]	DDR	DDR SDRAM0 data [28]
B3	DDR0_DQ[25]	DDR	DDR SDRAM0 data [25]
B4	DDR0_DQ[23]	DDR	DDR SDRAM0 data [23]
B5	DDR0_DQ[20]	DDR	DDR SDRAM0 data [20]
B6	DDR0_DQS_N[2]	DDR	DDR SDRAM0 Data Strobe DQS2_N
B7	DDR0_ADR[12]	DDR	DDR SDRAM0 Address [12]
B9	DDR0_ADR[6]	DDR	DDR SDRAM0 Address [6]
B10	DDR0_ADR[1]	DDR	DDR SDRAM0 Address [1]
B11	DDR0_ADR[10]	DDR	DDR SDRAM0 Address [10]
B12	DDR0_CK_N[1]	DDR	DDR SDRAM0 differential clock inputs CK1_N

Pin Number	Pin Name	IO-Type	Description
B14	DDR0_CK_N[0]	DDR	DDR SDRAM0 differential clock inputs CK0_N
B15	DDR0_PAR	DDR	DDR SDRAM0 PAR0
B16	DDR0_ATB1	DDR	DDR0 PHY IO pad Analog Test Bus (ATB)
B17	DDR0_CS_N[2]	DDR	DDR SDRAM0 CS2
B18	DDR0_RESET_N	DDR	DDR SDRAM0 Active Low Asynchronous Reset
B19	DDR0_DQ[14]	DDR	DDR SDRAM0 data [14]
B20	DDR0_DQS_P[1]	DDR	DDR SDRAM0 Data Strobe DQS1_P
B21	VSS	VSS	digital ground
B22	DDR0_DQ[5]	DDR	DDR SDRAM0 data [5]
B23	DDR0_DQS_P[0]	DDR	DDR SDRAM0 Data Strobe DQS0_P
B25	GPIO[20]	IO	function IO share with GPIO
B26	GPIO[19]	IO	function IO share with GPIO
B27	GPIO[22]	IO	function IO share with GPIO
B28	GPIO[25]	IO	function IO share with GPIO
B29	GPIO[24]	IO	function IO share with GPIO
B30	GPIO[27]	IO	function IO share with GPIO
B31	GPIO[31]	IO	function IO share with GPIO
C1	VSS	VSS	digital ground
C2	DDR0_DQ[31]	DDR	DDR SDRAM0 data [31]
C3	DDR0_DQS_N[3]	DDR	DDR SDRAM0 Data Strobe DQS3_N
C4	DDR0_DQ[27]	DDR	DDR SDRAM0 data [27]
C6	DDR0_DQ[21]	DDR	DDR SDRAM0 data [21]
C7	DDR0_DQ[18]	DDR	DDR SDRAM0 data [18]
C9	DDR0_ADR[9]	DDR	DDR SDRAM0 Address [9]
C10	DDR0_ADR[0]	DDR	DDR SDRAM0 Address [0]
C12	DDR0_ADR[8]	DDR	DDR SDRAM0 Address [8]
C14	DDR0_BA[0]	DDR	DDR SDRAM0 Bank Address 0
C16	DDR0_ERR_N	DDR	DDR SDRAM0 alert_n
C17	DDR0_CKE[0]	DDR	DDR SDRAM0 Clock0 enable
C19	DDR0_DM_DBI_N[1]	DDR	DDR SDRAM0 Input Data Mask and Data Bus Inversion for byte0

Pin Number	Pin Name	IO-Type	Description
C20	DDR0_DQ[9]	DDR	DDR SDRAM0 data [9]
C22	DDR0_DQ[4]	DDR	DDR SDRAM0 data [4]
C23	DDR0_DQS_N[0]	DDR	DDR SDRAM0 Data Strobe DQS0_N
C25	GPIO[2]	IO	function IO share with GPIO
C26	GPIO[33]	IO	function IO share with GPIO
C27	GPIO[35]	IO	function IO share with GPIO
C28	GPIO[37]	IO	function IO share with GPIO
C29	GPIO[40]	IO	function IO share with GPIO
C30	GPIO[45]	IO	function IO share with GPIO
C31	GPIO[44]	IO	function IO share with GPIO
D1	FUNC_SHARE[1]	IO	function IO share with group
D2	VSS	VSS	digital ground
D3	DDR0_DQS_P[3]	DDR	DDR SDRAM0 Data Strobe DQS3_P
D4	DDR0_DM_DBI_N[3]	DDR	DDR SDRAM0 Input Data Mask and Data Bus Inversion for byte0
D6	DDR0_DM_DBI_N[2]	DDR	DDR SDRAM0 Input Data Mask and Data Bus Inversion for byte0
D7	DDR0_DQ[17]	DDR	DDR SDRAM0 data [17]
D9	VSS	VSS	digital ground
D10	DDR0_ADR[3]	DDR	DDR SDRAM0 Address [3]
D12	DDR0_ADR[4]	DDR	DDR SDRAM0 Address [4]
D14	DDR0_RAS_N_ADR16	DDR	DDR SDRAM0 Address 16
D16	DDR0_PLL_REFOUT_N	DDR	DDR0 PHY Differential PLL reference clock output
D17	DDR0_ODT[0]	DDR	DDR SDRAM0 On Die Termination for CS0
D19	DDR0_DQ[13]	DDR	DDR SDRAM0 data [13]
D20	DDR0_DQ[11]	DDR	DDR SDRAM0 data [11]
D22	DDR0_DQ[2]	DDR	DDR SDRAM0 data [2]
D23	VSS	VSS	digital ground
D25	GPIO[5]	IO	function IO share with GPIO
D26	GPIO[8]	IO	function IO share with GPIO
D27	GPIO[48]	IO	function IO share with GPIO

Pin Number	Pin Name	IO-Type	Description
D28	GPIO[50]	IO	function IO share with GPIO
D29	GPIO[49]	IO	function IO share with GPIO
D30	GPIO[52]	IO	function IO share with GPIO
D31	GPIO[55]	IO	function IO share with GPIO
E1	FUNC_SHARE[0]	IO	function IO share with group
E2	VSS	VSS	digital ground
E6	DDR0_DQ[22]	DDR	DDR SDRAM0 data [22]
E7	DDR0_DQ[19]	DDR	DDR SDRAM0 data [19]
E9	DDR0_ADR[13]	DDR	DDR SDRAM0 Address [13]
E10	DDR0_ADR[5]	DDR	DDR SDRAM0 Address [5]
E12	DDR0_CAL	DDR	DDR0 PHY IO pad calibration resistor connection
E14	DDR0_CS_N[3]	DDR	DDR SDRAM0 CS3
E16	DDR0_PLL_REFOUT_P	DDR	DDR0 PHY Differential PLL reference clock output
E17	VSS	VSS	digital ground
E19	DDR0_DQ[12]	DDR	DDR SDRAM0 data [12]
E20	DDR0_DQ[10]	DDR	DDR SDRAM0 data [10]
E22	DDR0_DM_DBI_N[0]	DDR	DDR SDRAM0 Input Data Mask and Data Bus Inversion for byte0
E23	DDR0_DQ[1]	DDR	DDR SDRAM0 data [1]
E25	GPIO[10]	IO	function IO share with GPIO
E26	GPIO[14]	IO	function IO share with GPIO
E27	GPIO[21]	IO	function IO share with GPIO
E28	GPIO[23]	IO	function IO share with GPIO
E29	GPIO[54]	IO	function IO share with GPIO
E30	GPIO[57]	IO	function IO share with GPIO
E31	GPIO[60]	IO	function IO share with GPIO
F1	FUNC_SHARE[6]	IO	function IO share with group
F2	FUNC_SHARE[2]	IO	function IO share with group
F4	FUNC_SHARE[17]	IO	function IO share with group
F5	FUNC_SHARE[12]	IO	function IO share with group
F6	FUNC_SHARE[5]	IO	function IO share with group

Pin Number	Pin Name	IO-Type	Description
F7	VSS	VSS	digital ground
F9	DDR0_BG[1]	DDR	DDR SDRAM0 Bank Group1
F10	DDR0_ADR[7]	DDR	DDR SDRAM0 Address [7]
F12	DDR0_BA[1]	DDR	DDR SDRAM0 Bank Address 1
F14	DDR0_CAS_N_ADR15	DDR	DDR SDRAM0 Address 15
F16	VSS	VSS	digital ground
F17	DDR0_CKE[1]	DDR	DDR SDRAM0 Clock1 enable
F19	DDR0_CS_N[0]	DDR	DDR SDRAM0 CS0
F20	VSS	VSS	digital ground
F22	DDR0_DQ[3]	DDR	DDR SDRAM0 data [3]
F23	DDR0_DQ[0]	DDR	DDR SDRAM0 data [0]
F24	VSS	VSS	digital ground
F25	GPIO[11]	IO	function IO share with GPIO
F26	GPIO[18]	IO	function IO share with GPIO
F27	GPIO[16]	IO	function IO share with GPIO
F28	GPIO[26]	IO	function IO share with GPIO
F29	GPIO[59]	IO	function IO share with GPIO
F30	GPIO[62]	IO	function IO share with GPIO
F31	GPIO[61]	IO	function IO share with GPIO
G1	FUNC_SHARE[7]	IO	function IO share with group
G2	FUNC_SHARE[3]	IO	function IO share with group
G3	VSS	VSS	digital ground
G4	FUNC_SHARE[20]	IO	function IO share with group
G5	FUNC_SHARE[9]	IO	function IO share with group
G6	FUNC_SHARE[4]	IO	function IO share with group
G7	VDDQ_DDR0	DDR	DDR IO power
G8	VDDQ_DDR0	DDR	DDR IO power
G9	VDDQ_DDR0	DDR	DDR IO power
G10	VDDQ_DDR0	DDR	DDR IO power
G11	VDDQ_DDR0	DDR	DDR IO power
G12	DDR0_BG[0]	DDR	DDR SDRAM0 Bank Group0

Pin Number	Pin Name	IO-Type	Description
G13	VSS	VSS	digital ground
G14	DDR0_WE_N_ADR14	DDR	DDR SDRAM0 Address 14
G16	VSS	VSS	digital ground
G17	DDR0_ODT[1]	DDR	DDR SDRAM0 On Die Termination for CS1
G19	DDR0_PLL_TESTOUT_P	DDR	DDR0 PHY Differential PLL test clock output
G20	VSS	VSS	digital ground
G22	VSS	VSS	digital ground
G23	GPIO[4]	IO	function IO share with GPIO
G30	CDTX_L0N	MIPI	MIPI TX Lane-0 with the negative terminal
G31	CDTX_L0P	MIPI	MIPI TX Lane-0 with the positive terminal
H1	FUNC_SHARE[11]	IO	function IO share with group
H2	FUNC_SHARE[10]	IO	function IO share with group
H4	FUNC_SHARE[25]	IO	function IO share with group
H7	VSS	VSS	digital ground
H8	VDDQ_DDR0	DDR	MIPI TX Lane-3 with the negative terminal
H9	VSS	VSS	digital ground
H10	VSS	VSS	digital ground
H11	VDDQ_DDR0	DDR	MIPI TX Lane-4 with the positive terminal
H12	VDDQ_DDR0	DDR	DDR IO power
H13	VDDQ_DDR0	DDR	DDR IO power
H14	VDDQ_DDR0	DDR	DDR IO power
H15	VDDQ_DDR0	DDR	DDR IO power
H16	VSS	VSS	digital ground
H17	VSS	VSS	digital ground
H18	VSS	VSS	digital ground
H19	DDR0_PLL_TESTOUT_N	DDR	DDR0 PHY Differential PLL test clock output
H20	VSS	VSS	digital ground
H22	GPIO[1]	IO	function IO share with GPIO
H23	GPIO[7]	IO	function IO share with GPIO
H24	GPIO[13]	IO	function IO share with GPIO
H25	GPIO[28]	IO	function IO share with GPIO

Pin Number	Pin Name	IO-Type	Description
H26	GPIO[29]	IO	function IO share with GPIO
H27	GPIO[30]	IO	function IO share with GPIO
H28	GPIO[32]	IO	function IO share with GPIO
H29	GPIO[36]	IO	function IO share with GPIO
H30	CDTX_L1N	MIPI	MIPI TX Lane-1 with the negative terminal
H31	CDTX_L1P	MIPI	MIPI TX Lane-1 with the positive terminal
J1	FUNC_SHARE[22]	IO	function IO share with group
J2	FUNC_SHARE[18]	IO	function IO share with group
J3	FUNC_SHARE[15]	IO	function IO share with group
J4	FUNC_SHARE[14]	IO	function IO share with group
J5	FUNC_SHARE[24]	IO	function IO share with group
J6	FUNC_SHARE[16]	IO	function IO share with group
J7	FUNC_SHARE[8]	IO	function IO share with group
J9	VSS	VSS	digital ground
J10	VSS	VSS	digital ground
J11	VDDQ_DDR0	DDR	DDR IO power
J12	VSS	VSS	digital ground
J13	VDDQ_DDR0	DDR	DDR IO power
J14	VDDQ_DDR0	DDR	DDR IO power
J15	VDDQ_DDR0	DDR	DDR IO power
J16	VSS	VSS	digital ground
J17	VSS	VSS	digital ground
J18	VDDQ_DDR0	DDR	DDR IO power
J19	VDDQ_DDR0	DDR	DDR IO power
J20	VDDQ_DDR0	DDR	DDR IO power
J22	VSS	VSS	digital ground
J23	VSS	VSS	digital ground
J25	GPIO[34]	IO	function IO share with GPIO
J26	GPIO[38]	IO	function IO share with GPIO
J27	GPIO[41]	IO	function IO share with GPIO
J28	GPIO[39]	IO	function IO share with GPIO

Pin Number	Pin Name	IO-Type	Description
J29	GPIO[42]	IO	function IO share with GPIO
J30	CDTX_L2N	MIPI	MIPI TX Lane-2 with the negative terminal
J31	CDTX_L2P	MIPI	MIPI TX Lane-2 with the positive terminal
K1	FUNC_SHARE[27]	IO	function IO share with group
K2	FUNC_SHARE[23]	IO	function IO share with group
K3	VSS	VSS	digital ground
K4	FUNC_SHARE[19]	IO	function IO share with group
K5	VSS	VSS	digital ground
K6	FUNC_SHARE[21]	IO	function IO share with group
K7	FUNC_SHARE[13]	IO	function IO share with group
K8	VSS	VSS	digital ground
K9	VSS	VSS	digital ground
K10	VSS	VSS	digital ground
K11	VSS	VSS	digital ground
K12	VDDQ_DDR0	DDR	DDR IO power
K13	VDDQ_DDR0	DDR	DDR IO power
K14	VDDQ_DDR0	DDR	DDR IO power
K15	VDDQ_DDR0	DDR	DDR IO power
K16	VDDQ_DDR0	DDR	DDR IO power
K17	VDDQ_DDR0	DDR	DDR IO power
K18	VDDQ_DDR0	DDR	DDR IO power
K19	VDDQ_DDR0	DDR	DDR IO power
K22	VSS	VSS	digital ground
K23	VSS	VSS	digital ground
K25	VSS	VSS	digital ground
K30	CDTX_L3N	MIPI	MIPI TX Lane-3 with the negative terminal
K31	CDTX_L3P	MIPI	MIPI TX Lane-3 with the positive terminal
L1	FUNC_SHARE[26]	IO	function IO share with group
L8	VSS	VSS	digital ground
L9	VSS	VSS	digital ground
L10	VSS	VSS	digital ground

Pin Number	Pin Name	IO-Type	Description
L11	VSS	VSS	digital ground
L12	VSS	VSS	digital ground
L13	VSS	VSS	digital ground
L14	VDDQ_DDR0	DDR	DDR IO power
L15	VDDQCK_DDR0	DDR	DDR CK power
L16	VSS	VSS	digital ground
L17	VDDPLL_DDR0	DDR	DDR PLL power
L18	VSS	VSS	digital ground
L19	VSS	VSS	digital ground
L20	VSS	VSS	digital ground
L21	VDD	VDD	digital core power
L22	VSS	VSS	digital ground
L23	VSS	VSS	digital ground
L25	GPIO[43]	IO	function IO share with GPIO
L26	GPIO[46]	IO	function IO share with GPIO
L27	GPIO[47]	IO	function IO share with GPIO
L28	GPIO[51]	IO	function IO share with GPIO
L29	EXT_RSTN	IO	chip reset, low active
L30	CDTX_L4N	MIPI	MIPI TX Lane-4 with the negative terminal
L31	CDTX_L4P	MIPI	MIPI TX Lane-4 with the positive terminal
M1	FUNC_SHARE[35]	IO	function IO share with group
M2	FUNC_SHARE[34]	IO	function IO share with group
M3	FUNC_SHARE[31]	IO	function IO share with group
M4	FUNC_SHARE[30]	IO	function IO share with group
M5	FUNC_SHARE[32]	IO	function IO share with group
M6	FUNC_SHARE[28]	IO	function IO share with group
M7	FUNC_SHARE[29]	IO	function IO share with group
M8	VDD18	VDDIO	digital IO power
M9	VDD18	VDDIO	digital IO power
M10	VSS	VSS	digital ground
M11	VSS	VSS	digital ground

Pin Number	Pin Name	IO-Type	Description
M12	VSS	VSS	digital ground
M13	VSS	VSS	digital ground
M14	VSS	VSS	digital ground
M15	VSS	VSS	digital ground
M16	VSS	VSS	digital ground
M17	VSS	VSS	digital ground
M18	VSS	VSS	digital ground
M19	VDD	VDD	digital core power
M20	VSS	VSS	digital ground
M21	VDD	VDD	digital core power
M22	VSS	VSS	digital ground
M23	AVDD18_MIPITX	AVDD18	MIPI TX analog power
M24	VSS	VSS	digital ground
M25	GPIO[53]	IO	function IO share with GPIO
M26	GPIO[56]	IO	function IO share with GPIO
M27	GPIO[58]	IO	function IO share with GPIO
M28	GPIO[63]	IO	function IO share with GPIO
M29	TEST_MODE	IO	test mode enable for DFT, high active
M30	CSI2RX_DN5	MIPI	MIPI CSI RX Lane-5 with the negative terminal
M31	CSI2RX_DP5	MIPI	MIPI CSI RX Lane-5 with the positive terminal
N1	FUNC_SHARE[43]	IO	function IO share with group
N2	FUNC_SHARE[38]	IO	function IO share with group
N3	VSS	VSS	digital ground
N4	FUNC_SHARE[39]	IO	function IO share with group
N5	FUNC_SHARE[37]	IO	function IO share with group
N6	FUNC_SHARE[36]	IO	function IO share with group
N7	FUNC_SHARE[33]	IO	function IO share with group
N8	VDD18	VDDIO	digital IO power
N9	VDD18	VDDIO	digital IO power
N10	VDD18	VDDIO	digital IO power
N11	VDD18	VDDIO	digital IO power

Pin Number	Pin Name	IO-Type	Description
N12	VSS	VSS	digital ground
N13	VDD3318_CHIPLINK	VDD3318	FUNC_SHARE[0-69] IO power
N14	VDD3318_CHIPLINK	VDD3318	FUNC_SHARE[0-69] IO power
N15	VSS	VSS	digital ground
N16	VSS	VSS	digital ground
N17	VSS	VSS	digital ground
N18	VSS	VSS	digital ground
N19	VDD	VDD	digital core power
N20	VSS	VSS	digital ground
N21	VDD	VDD	digital core power
N22	VSS	VSS	digital ground
N24	AVSS_MIPIRX	AVSS	MIPI RX analog ground
N25	VSS	VSS	digital ground
N30	CSI2RX_DN4	MIPI	MIPI CSI RX Lane-4 with the negative terminal
N31	CSI2RX_DP4	MIPI	MIPI CSI RX Lane-4 with the positive terminal
P1	FUNC_SHARE[42]	IO	function IO share with group
P8	VDD18	VDDIO	digital IO power
P9	VDD18	VDDIO	digital IO power
P10	VDD18	VDDIO	digital IO power
P11	VDD18	VDDIO	digital IO power
P12	VSS	VSS	digital ground
P13	VDD3318_CHIPLINK	VDD3318	FUNC_SHARE[0-69] IO power
P14	VSS	VSS	digital ground
P15	VSS	VSS	digital ground
P16	VDD	VDD	digital core power
P17	VDD	VDD	digital core power
P18	VSS	VSS	digital ground
P19	VDD	VDD	digital core power
P20	VSS	VSS	digital ground
P21	VDD	VDD	digital core power
P22	VSS	VSS	digital ground

Pin Number	Pin Name	IO-Type	Description
P23	AVDD09_MIPIRX	AVDD	MIPI RX analog power
P24	VSS	VSS	digital ground
P25	QSPI_DATA[3]	IO	QSPI serial data [3]
P26	QSPI_DATA[2]	IO	QSPI serial data [2]
P27	QSPI_CSN0	IO	SPI Flash chip select 0, low active
P28	FUNC_SHARE[130]	IO	function IO share with group
P29	FUNC_SHARE[136]	IO	function IO share with group
P30	CSI2RX_DN3	MIPI	MIPI CSI RX Lane-3 with the negative terminal
P31	CSI2RX_DP3	MIPI	MIPI CSI RX Lane-3 with the positive terminal
R1	FUNC_SHARE[50]	IO	function IO share with group
R2	FUNC_SHARE[47]	IO	function IO share with group
R3	FUNC_SHARE[46]	IO	function IO share with group
R4	FUNC_SHARE[45]	IO	function IO share with group
R5	FUNC_SHARE[44]	IO	function IO share with group
R6	FUNC_SHARE[41]	IO	function IO share with group
R7	FUNC_SHARE[40]	IO	function IO share with group
R8	VDD18	VDDIO	digital IO power
R9	VDD18	VDDIO	digital IO power
R10	VDD18	VDDIO	digital IO power
R11	VDD18	VDDIO	digital IO power
R12	VSS	VSS	digital ground
R13	VDD3318_CHIPLINK	VDD3318	FUNC_SHARE[0-69] IO power
R14	VSS	VSS	digital ground
R15	VSS	VSS	digital ground
R16	VDD	VDD	digital core power
R17	VDD	VDD	digital core power
R18	VDD	VDD	digital core power
R19	VDD	VDD	digital core power
R20	VSS	VSS	digital ground
R21	VDD	VDD	digital core power
R22	VSS	VSS	digital ground

Pin Number	Pin Name	IO-Type	Description
R23	VSS	VSS	digital ground
R25	QSPI_CLK	IO	SPI NAND/NOR Flash device clock
R26	QSPI_DATA[0]	IO	QSPI serial data [0]
R27	QSPI_DATA[1]	IO	QSPI serial data [1]
R28	FUNC_SHARE[140]	IO	function IO share with group
R29	FUNC_SHARE[118]	IO	function IO share with group
R30	CSI2RX_DN2	MIPI	MIPI CSI RX Lane-2 with the negative terminal
R31	CSI2RX_DP2	MIPI	MIPI CSI RX Lane-2 with the positive terminal
T1	FUNC_SHARE[51]	IO	function IO share with group
T2	FUNC_SHARE[52]	IO	function IO share with group
T3	VSS	VSS	digital ground
T4	FUNC_SHARE[55]	IO	function IO share with group
T5	FUNC_SHARE[53]	IO	function IO share with group
T6	FUNC_SHARE[49]	IO	function IO share with group
T7	FUNC_SHARE[48]	IO	function IO share with group
T9	VSS	VSS	digital ground
T10	VSS	VSS	digital ground
T11	VSS	VSS	digital ground
T12	VSS	VSS	digital ground
T13	VDD3318_CHIPLINK	VDD3318	FUNC_SHARE[0-69] IO power
T14	VSS	VSS	digital ground
T15	VDD	VDD	digital core power
T16	VDD	VDD	digital core power
T17	VDD	VDD	digital core power
T18	VDD	VDD	digital core power
T19	VDD	VDD	digital core power
T20	VDD	VDD	digital core power
T21	VDD	VDD	digital core power
T22	VSS	VSS	digital ground
T23	AVDD18_MIPIRX	AVDD18	MIPI RX analog power supply for LDO
T24	VSS	VSS	digital ground

Pin Number	Pin Name	IO-Type	Description
T25	VSS	VSS	digital ground
T30	CSI2RX_DN1	MIPI	MIPI CSI RX Lane-1 with the negative terminal
T31	CSI2RX_DP1	MIPI	MIPI CSI RX Lane-1 with the positive terminal
U1	FUNC_SHARE[54]	IO	function IO share with group
U8	VSS	VSS	digital ground
U9	VSS	VSS	digital ground
U10	VSS	VSS	digital ground
U11	VSS	VSS	digital ground
U12	VSS	VSS	digital ground
U13	VSS	VSS	digital ground
U14	VDD	VDD	digital core power
U15	VDD	VDD	digital core power
U16	VDD	VDD	digital core power
U17	VDD	VDD	digital core power
U18	VSS	VSS	digital ground
U19	VSS	VSS	digital ground
U20	AVSS_PLL0	AVSS	PLL0 analog ground
U21	AVDD09_PLL0	AVDD	PLL0 analog power
U22	AVDD09_PLL1	AVDD	PLL1 analog power
U23	AVSS_PLL1	AVSS	PLL1 analog ground
U24	ANA18_TEMP_TEST1	AIO	Analog test access
U25	ANA18_TEMP_TEST0	AIO	Analog test access
U26	FUNC_SHARE[137]	IO	function IO share with group
U27	FUNC_SHARE[138]	IO	function IO share with group
U28	FUNC_SHARE[132]	IO	function IO share with group
U29	FUNC_SHARE[116]	IO	function IO share with group
U30	CSI2RX_DN0	MIPI	MIPI CSI RX Lane-0 with the negative terminal
U31	CSI2RX_DP0	MIPI	MIPI CSI RX Lane-0 with the positive terminal
V1	FUNC_SHARE[56]	IO	function IO share with group
V2	FUNC_SHARE[57]	IO	function IO share with group
V3	FUNC_SHARE[60]	IO	function IO share with group

Pin Number	Pin Name	IO-Type	Description
V4	FUNC_SHARE[61]	IO	function IO share with group
V5	FUNC_SHARE[59]	IO	function IO share with group
V6	FUNC_SHARE[58]	IO	function IO share with group
V7	FUNC_SHARE[63]	IO	function IO share with group
V8	VDD3318_LCD	VDD3318	FUNC_SHARE[70-97] IO power
V9	VDD3318_LCD	VDD3318	FUNC_SHARE[70-97] IO power
V10	VSS	VSS	digital ground
V11	VSS	VSS	digital ground
V12	VSS	VSS	digital ground
V13	VSS	VSS	digital ground
V14	VDD	VDD	digital core power
V15	VDD	VDD	digital core power
V16	VDD	VDD	digital core power
V17	VDD	VDD	digital core power
V18	VSS	VSS	digital ground
V19	VSS	VSS	digital ground
V20	AVSS_PLL2	AVSS	PLL2 analog ground
V21	AVDD09_PLL2	AVDD	PLL2 analog power
V24	ANA18_TEMP_VSS	AIO	Ground sense, VSS return output
V25	ANA18_TEMP_VCAL	AIO	Calibration voltage input,700mV±20mV
V26	FUNC_SHARE[133]	IO	function IO share with group
V27	FUNC_SHARE[127]	IO	function IO share with group
V28	FUNC_SHARE[131]	IO	function IO share with group
V29	FUNC_SHARE[122]	IO	function IO share with group
V30	OSC1_XIN	OSC	27MHz crystal input
V31	OSC1_XOUT	OSC	27MHz crystal output
W1	FUNC_SHARE[64]	IO	function IO share with group
W2	FUNC_SHARE[65]	IO	function IO share with group
W3	VSS	VSS	digital ground
W4	FUNC_SHARE[68]	IO	function IO share with group

Pin Number	Pin Name	IO-Type	Description
W5	FUNC_SHARE[62]	IO	function IO share with group
W6	FUNC_SHARE[67]	IO	function IO share with group
W7	FUNC_SHARE[66]	IO	function IO share with group
W8	VDD3318_LCD	VDD3318	FUNC_SHARE[70-97] IO power
W9	VDD3318_LCD	VDD3318	FUNC_SHARE[70-97] IO power
W10	VSS	VSS	digital ground
W11	VDD	VDD	digital core power
W12	VSS	VSS	digital ground
W13	VSS	VSS	digital ground
W14	VDD	VDD	digital core power
W15	VDD	VDD	digital core power
W16	VDD	VDD	digital core power
W17	VDD	VDD	digital core power
W18	VDD	VDD	digital core power
W19	VDD	VDD	digital core power
W20	VSS	VSS	digital ground
W21	VSS	VSS	digital ground
W23	AVDD18_TS	AVDD18	Temperature sensor analog power
W24	VSS18_TS	VSS	Temperature sensor analog ground
W25	VSS	VSS	digital ground
W27	FUNC_SHARE[126]	IO	function IO share with group
W28	FUNC_SHARE[123]	IO	function IO share with group
W30	VSS	VSS	digital ground
W31	VSS	VSS	digital ground
Y1	FUNC_SHARE[69]	IO	function IO share with group
Y2	FUNC_SHARE[73]	IO	function IO share with group
Y8	VSS	VSS	digital ground
Y9	VSS	VSS	digital ground
Y10	VSS	VSS	digital ground
Y11	VDD	VDD	digital core power
Y12	VDD	VDD	digital core power

Pin Number	Pin Name	IO-Type	Description
Y13	VDD	VDD	digital core power
Y14	VSS	VSS	digital ground
Y15	VDD	VDD	digital core power
Y16	VSS	VSS	digital ground
Y17	VSS	VSS	digital ground
Y18	VSS	VSS	digital ground
Y19	VSS	VSS	digital ground
Y20	VSS	VSS	digital ground
Y21	VDD3318_GMII	VDD3318	FUNC_SHARE[115-141] IO power
Y25	FUNC_SHARE[129]	IO	function IO share with group
Y26	FUNC_SHARE[134]	IO	function IO share with group
Y27	FUNC_SHARE[135]	IO	function IO share with group
Y28	FUNC_SHARE[139]	IO	function IO share with group
Y29	FUNC_SHARE[141]	IO	function IO share with group
Y30	OSC0_XIN	OSC	25MHz crystal input
Y31	OSC0_XOUT	OSC	25MHz crystal output

9.2 Package Ball Map

The following figure shows the package ball map:

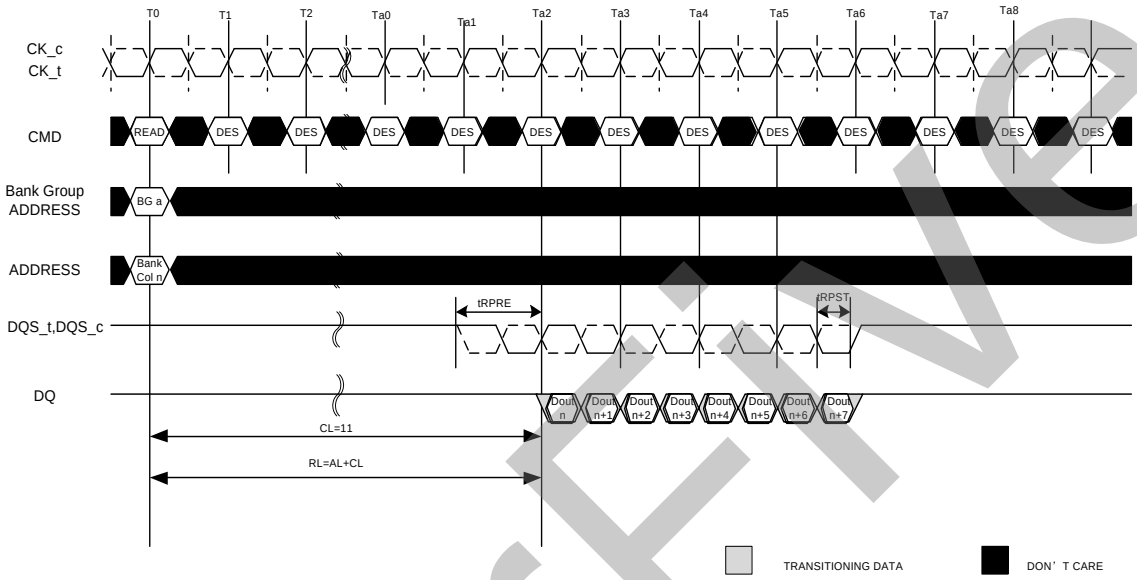
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
A	DDR0_DQ[30]	DDR0_DQ[24]	DDR0_DQ[26]	VSS	DDR0_DQ[16]	DDR0_DQS_P[2]	VSS		DDR0_ACT_N	DDR0_ADR[11]	VSS	DDR0_CK_P[1]		DDR0_CK_P[0]	DDR0_ADR[2]	DDR0_ATB0	DDR0_CS_N[1]	VSS	DDR0_DQ[15]	DDR0_DQS_N[1]	DDR0_DQ[8]	DDR0_DQ[7]	DDR0_DQ[6]		GPIO[0]	GPIO[3]	GPIO[6]	GPIO[9]	GPIO[12]	GPIO[15]	GPIO[17]
B	DDR0_DQ[29]	DDR0_DQ[28]	DDR0_DQ[25]	DDR0_DQ[23]	DDR0_DQ[20]	DDR0_DQS_N[2]	DDR0_ADR[12]		DDR0_ADR[6]	DDR0_ADR[1]	DDR0_ADR[10]	DDR0_CK_N[1]		DDR0_CK_N[0]	DDR0_PAR	DDR0_ATB1	DDR0_CS_N[2]	DDR0_RESET_N	DDR0_DQ[14]	DDR0_DQS_P[1]	VSS	DDR0_DQ[5]	DDR0_DQS_P[0]		GPIO[20]	GPIO[19]	GPIO[22]	GPIO[25]	GPIO[24]	GPIO[27]	GPIO[31]
C	VSS	DDR0_DQ[31]	DDR0_DQS_N[3]	DDR0_DQ[27]		DDR0_DQ[21]	DDR0_DQ[18]		DDR0_ADR[9]	DDR0_ADR[0]		DDR0_ADR[8]		DDR0_BA[0]		DDR0_ERR_N	DDR0_CKE[0]		DDR0_DM_DBI_N[1]	DDR0_DQ[9]		DDR0_DQ[4]	DDR0_DQS_N[0]		GPIO[2]	GPIO[33]	GPIO[35]	GPIO[37]	GPIO[40]	GPIO[45]	GPIO[44]
D	FUNC_SHARE[1]	VSS	DDR0_DQS_P[3]	DDR0_DM_DBI_N[3]		DDR0_DM_DBI_N[2]	DDR0_DQ[17]		VSS	DDR0_ADR[3]		DDR0_ADR[4]		DDR0_RAS_N_ADR16		DDR0_PLL_REFOUT_N	DDR0_ODT[0]		DDR0_DQ[13]	DDR0_DQ[11]		DDR0_DQ[2]	VSS		GPIO[5]	GPIO[8]	GPIO[48]	GPIO[50]	GPIO[49]	GPIO[52]	GPIO[55]
E	FUNC_SHARE[0]	VSS				DDR0_DQ[22]	DDR0_DQ[19]		DDR0_ADR[13]	DDR0_ADR[5]		DDR0_CAL		DDR0_CS_N[3]		DDR0_PLL_REFOUT_P	VSS		DDR0_DQ[12]	DDR0_DQ[10]		DDR0_DM_DBI_N[0]	DDR0_DQ[1]		GPIO[10]	GPIO[14]	GPIO[21]	GPIO[23]	GPIO[54]	GPIO[57]	GPIO[60]
F	FUNC_SHARE[6]	FUNC_SHARE[2]		FUNC_SHARE[17]	FUNC_SHARE[12]	FUNC_SHARE[5]	VSS		DDR0_BG[1]	DDR0_ADR[7]		DDR0_BA[1]		DDR0_CAS_N_ADR15		VSS	DDR0_CKE[1]		DDR0_CS_N[0]	VSS		DDR0_DQ[3]	DDR0_DQ[0]	VSS	GPIO[11]	GPIO[18]	GPIO[16]	GPIO[26]	GPIO[59]	GPIO[62]	GPIO[61]
G	FUNC_SHARE[7]	FUNC_SHARE[3]	VSS	FUNC_SHARE[20]	FUNC_SHARE[9]	FUNC_SHARE[4]	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	DDR0_BG[0]	VSS	DDR0_WE_N_ADR14		VSS	DDR0_ODT[1]		DDR0_PLL_TESTOUT_P	VSS		VSS	GPIO[4]						CDTX_L0N	CDTX_L0P
H	FUNC_SHARE[11]	FUNC_SHARE[10]		FUNC_SHARE[25]			VSS	VDDQ_DDR0	VSS	VSS	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VSS	VSS	VSS	DDR0_PLL_TESTOUT_N	VSS		GPIO[1]	GPIO[7]	GPIO[13]	GPIO[28]	GPIO[29]	GPIO[30]	GPIO[32]	GPIO[36]	CDTX_L1N	CDTX_L1P
J	FUNC_SHARE[22]	FUNC_SHARE[18]	FUNC_SHARE[15]	FUNC_SHARE[14]	FUNC_SHARE[24]	FUNC_SHARE[16]	FUNC_SHARE[8]		VSS	VSS	VDDQ_DDR0	VSS	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VSS	VSS	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0		VSS	VSS		GPIO[34]	GPIO[38]	GPIO[41]	GPIO[39]	GPIO[42]	CDTX_L2N	CDTX_L2P
K	FUNC_SHARE[27]	FUNC_SHARE[23]	VSS	FUNC_SHARE[19]	VSS	FUNC_SHARE[21]	FUNC_SHARE[13]	VSS	VSS	VSS	VSS	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0			VSS	VSS		VSS					CDTX_L3N	CDTX_L3P
L	FUNC_SHARE[26]							VSS	VSS	VSS	VSS	VSS	VSS	VDDQ_DDR0	VDDQCK_DDR0	VSS	VDDPLL_DDR0	VSS	VSS	VSS	VDD	VSS	VSS		GPIO[43]	GPIO[46]	GPIO[47]	GPIO[51]	EXT_RSTN	CDTX_L4N	CDTX_L4P
M	FUNC_SHARE[35]	FUNC_SHARE[34]	FUNC_SHARE[31]	FUNC_SHARE[30]	FUNC_SHARE[32]	FUNC_SHARE[28]	FUNC_SHARE[29]	VDD18	VDD18	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VSS	VDD	VSS	AVDD18_MIPITX	VSS	GPIO[53]	GPIO[56]	GPIO[58]	GPIO[63]	TEST_MODE	CSI2RX_DN5	CSI2RX_DP5
N	FUNC_SHARE[43]	FUNC_SHARE[38]	VSS	FUNC_SHARE[39]	FUNC_SHARE[37]	FUNC_SHARE[36]	FUNC_SHARE[33]	VDD18	VDD18	VDD18	VDD18	VSS	VDD3318_CHIPLINK	VDD3318_CHIPLINK	VSS	VSS	VSS	VSS	VDD	VSS	VDD	VSS		AVSS_MIPIRX	VSS					CSI2RX_DN4	CSI2RX_DP4
P	FUNC_SHARE[42]							VDD18	VDD18	VDD18	VDD18	VSS	VDD3318_CHIPLINK	VSS	VSS	VDD	VDD	VSS	VDD	VSS	VDD	VSS	AVDD09_MIPIRX	VSS	QSPI_DATA[3]	QSPI_DATA[2]	QSPI_CSN0	FUNC_SHARE[130]	FUNC_SHARE[136]	CSI2RX_DN3	CSI2RX_DP3
R	FUNC_SHARE[50]	FUNC_SHARE[47]	FUNC_SHARE[46]	FUNC_SHARE[45]	FUNC_SHARE[44]	FUNC_SHARE[41]	FUNC_SHARE[40]	VDD18	VDD18	VDD18	VDD18	VSS	VDD3318_CHIPLINK	VSS	VSS	VDD	VDD	VDD	VDD	VSS	VDD	VSS	VSS		QSPI_CLK	QSPI_DATA[0]	QSPI_DATA[1]	FUNC_SHARE[140]	FUNC_SHARE[118]	CSI2RX_DN2	CSI2RX_DP2
T	FUNC_SHARE[51]	FUNC_SHARE[52]	VSS	FUNC_SHARE[55]	FUNC_SHARE[53]	FUNC_SHARE[49]	FUNC_SHARE[48]		VSS	VSS	VSS	VSS	VDD3318_CHIPLINK	VSS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	AVDD18_MIPIRX	VSS	VSS						CSI2RX_DN1	CSI2RX_DP1
U	FUNC_SHARE[54]							VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VSS	VSS	AVSS_PLL0	AVDD09_PLL0	AVDD09_PLL1	AVSS_PLL1	ANA18_TEMP_TEST1	ANA18_TEMP_TEST0	FUNC_SHARE[137]	FUNC_SHARE[138]	FUNC_SHARE[132]	FUNC_SHARE[116]	CSI2RX_DN0	CSI2RX_DP0
V	FUNC_SHARE[56]	FUNC_SHARE[57]	FUNC_SHARE[60]	FUNC_SHARE[61]	FUNC_SHARE[59]	FUNC_SHARE[58]	FUNC_SHARE[63]	VDD3318_LCD	VDD3318_LCD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VSS	VSS	AVSS_PLL2	AVDD09_PLL2			ANA18_TEMP_VSS	ANA18_TEMP_VCAL	FUNC_SHARE[133]	FUNC_SHARE[127]	FUNC_SHARE[131]	FUNC_SHARE[122]	OSC1_XIN	OSC1_XOUT
W	FUNC_SHARE[64]	FUNC_SHARE[65]	VSS	FUNC_SHARE[68]	FUNC_SHARE[62]	FUNC_SHARE[67]	FUNC_SHARE[66]	VDD3318_LCD	VDD3318_LCD	VSS	VDD	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS		AVDD18_TS	VSS18_TS	VSS		FUNC_SHARE[126]	FUNC_SHARE[123]		VSS	VSS
Y	FUNC_SHARE[69]	FUNC_SHARE[73]						VSS	VSS	VSS	VDD	VDD	VDD	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD3318_GMII				FUNC_SHARE[129]	FUNC_SHARE[134]	FUNC_SHARE[135]	FUNC_SHARE[139]	FUNC_SHARE[141]	OSC0_XIN	OSC0_XOUT
AA	FUNC_SHARE[72]	FUNC_SHARE[77]	FUNC_SHARE[70]	FUNC_SHARE[71]	FUNC_SHARE[74]	FUNC_SHARE[75]		VSS	VDD3318_SENSOR	VSS	VDD	VSS	VSS	VSS	VSS	VDDQCK_DDR1	VSS	VDDPLL_DDR1	VSS	VSS	VDD3318_GMII	VSS	AVDD33_USB	AVSS_USB	FUNC_SHARE[121]	FUNC_SHARE[120]	FUNC_SHARE[115]	FUNC_SHARE[124]	VSS	FUNC_SHARE[125]	FUNC_SHARE[128]
AB	FUNC_SHARE[76]	FUNC_SHARE[81]	VSS	FUNC_SHARE[85]	FUNC_SHARE[78]	FUNC_SHARE[79]	FUNC_SHARE[82]	VSS	VDD3318_SENSOR	VSS	VSS	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VSS	VDDQ_DDR1	VSS	VSS	DVDD18_OTP	VSS18_OTP								FUNC_SHARE[117]	FUNC_SHARE[119]
AC	FUNC_SHARE[80]							VSS	VSS	VSS	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VSS	VSS	VDDQ_DDR1	VSS	VDDQ_DDR1	VSS	VSS	ANA18_OTP_PENVDD2	VSS	AVDD09TX_USB	AVSSTX_USB	VSS	USB_SSTXB1	USB_SSTXA1	USB_DP	USB_DM	USB_SSRXB2	USB_SSRXA2
AD	FUNC_SHARE[84]	FUNC_SHARE[89]	FUNC_SHARE[92]	FUNC_SHARE[96]	FUNC_SHARE[97]	FUNC_SHARE[102]	FUNC_SHARE[101]	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VSS	VSS	VSS	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VSS	VSS	VSS	VSS	AVDD09RX_USB	AVDD18_USB	VSS	USB_SSRXB1	USB_SSRXA1	VSS	VSS	USB_SSTXA2	USB_SSTXB2
AE	FUNC_SHARE[88]	FUNC_SHARE[93]	VSS	FUNC_SHARE[94]	FUNC_SHARE[104]	FUNC_SHARE[108]	FUNC_SHARE[112]	VSS	VDDQ_DDR1	VDDQ_DDR1	VSS	VDDQ_DDR1	DDR1_ADR[9]	VSS	VSS	DDR1_BG[0]	VDDQ_DDR1	DDR1_CAS_N_ADR15	VDDQ_DDR1	VSS	VDDQ_DDR1	VDDQ_DDR1	AVSSRX_USB	VSS							VSS
AF	FUNC_SHARE[99]						DDR1_DQ[31]	DDR1_DQ[28]		DDR1_DQ[23]	DDR1_DQ[22]		DDR1_ADR[6]	DDR1_ADR[3]		DDR1_BA[1]		DDR1_WE_N_ADR14		DDR1_CS_N[3]	DDR1_PLL_REFOUT_N		DDR1_DQ[15]	DDR1_DQ[14]		DDR1_DQ[8]	VSS		DDR1_DQ[0]	DDR1_DQ[3]	
AG	FUNC_SHARE[100]	FUNC_SHARE[83]	FUNC_SHARE[87]	FUNC_SHARE[91]	VSS		DDR1_DQ[30]	DDR1_DQ[29]		DDR1_DQ[20]	DDR1_DM_DBI_N[2]			DDR1_ADR[5]		DDR1_ADR[0]		VSS		DDR1_CAL	DDR1_PLL_REFOUT_P		DDR1_CKE[0]	VSS		DDR1_DQ[11]	DDR1_DQ[10]		DDR1_DQ[1]	DDR1_DM_DBI_N[0]	
AH	FUNC_SHARE[103]	FUNC_SHARE[86]	VSS	FUNC_SHARE[95]	FUNC_SHARE[106]		VSS	DDR1_DM_DBI_N[3]		VSS	DDR1_DQ[21]		VSS	DDR1_ADR[7]		VSS		DDR1_PAR		DDR1_CS_N[2]	DDR1_CS_N[1]		DDR1_ODT[1]	DDR1_ODT[0]		VSS	DDR1_DQ[9]		VSS	DDR1_DQ[2]	
AJ	FUNC_SHARE[105]						DDR1_DQS_P[3]	DDR1_DQ[27]		DDR1_DQS_N[2]	DDR1_DQ[19]	DDR1_BG[1]	DDR1_ADR[12]	DDR1_ADR[10]		DDR1_ADR[2]		DDR1_ADR[1]		DDR1_ERR_N	VSS		VSS	DDR1_CKE[1]		DDR1_DM_DBI_N[1]	DDR1_DQS_P[1]		DDR1_DQ[4]	DDR1_DQS_N[0]	
AK	FUNC_SHARE[107]	FUNC_SHARE[109]	VSS	FUNC_SHARE[98]	VSS		DDR1_DQS_N[3]	DDR1_DQ[26]		DDR1_DQS_P[2]	DDR1_DQ[17]	DDR1_ADR[13]	DDR1_ACT_N	DDR1_ADR[8]		DDR1_CK_N[1]		DDR1_CK_N[0]		DDR1_RAS_N_ADR16	DDR1_ATB0		DDR1_CS_N[0]	DDR1_PLL_TESTOUT_N		VSS	DDR1_DQS_N[1]		DDR1_DQ[5]	DDR1_DQS_P[0]	
AL	FUNC_SHARE[111]	FUNC_SHARE[113]	FUNC_SHARE[90]	FUNC_SHARE[110]	FUNC_SHARE[114]	VSS	DDR1_DQ[25]	DDR1_DQ[24]	VSS	DDR1_DQ[18]	DDR1_DQ[16]	VSS	DDR1_ADR[11]	DDR1_ADR[4]	VSS	DDR1_CK_P[1]		DDR1_CK_P[0]	VSS	DDR1_BA[0]	DDR1_ATB1	VSS	DDR1_RESET_N	DDR1_PLL_TESTOUT_P	VSS	DDR1_DQ[13]	DDR1_DQ[12]	VSS	DDR1_DQ[7]	DDR1_DQ[6]	

Figure 9-1 Package Ball Map

10 Interface and AC Timing

10.1 DDR Interface and Timing

- DDR4/DDR3
  - READ Burst Operation RL=11(AL=0, CL=11, BL8)



NOTE1 BL=8,AL=0,CL=11,Preamble=1tCK

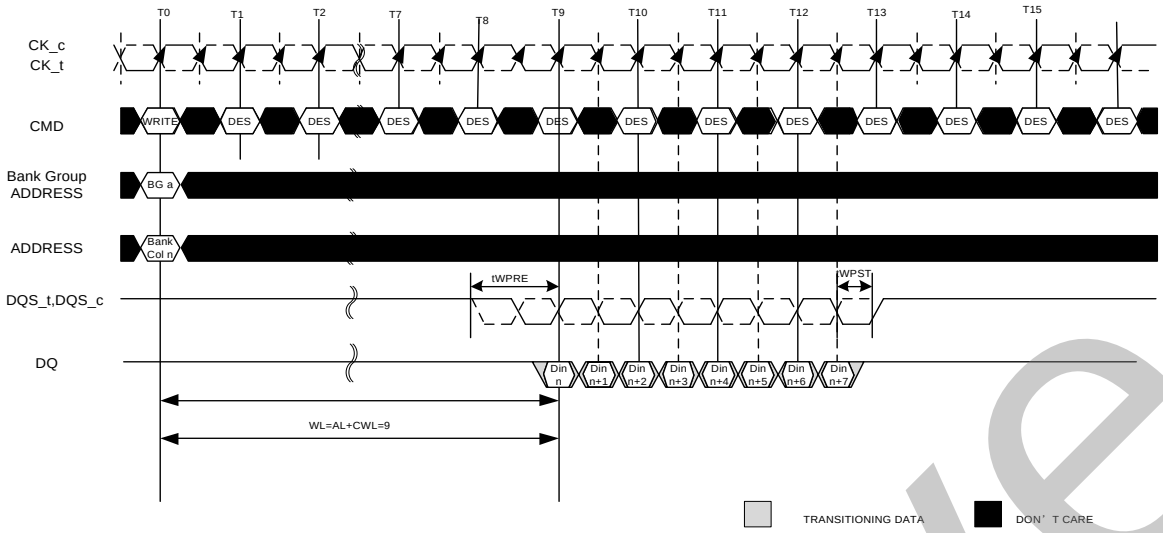
NOTE2 DOUTn=data-out from column n.

NOTE3 DES commands are shown for ease of illustration;other commands may be valid at these times.

NOTE4 BL8 setting activated by either MR0[A1:0=00]or MR0[A1:0=01]and A12=1 during READ command at T0.

Figure 10-1 DDR Read Burst Operation

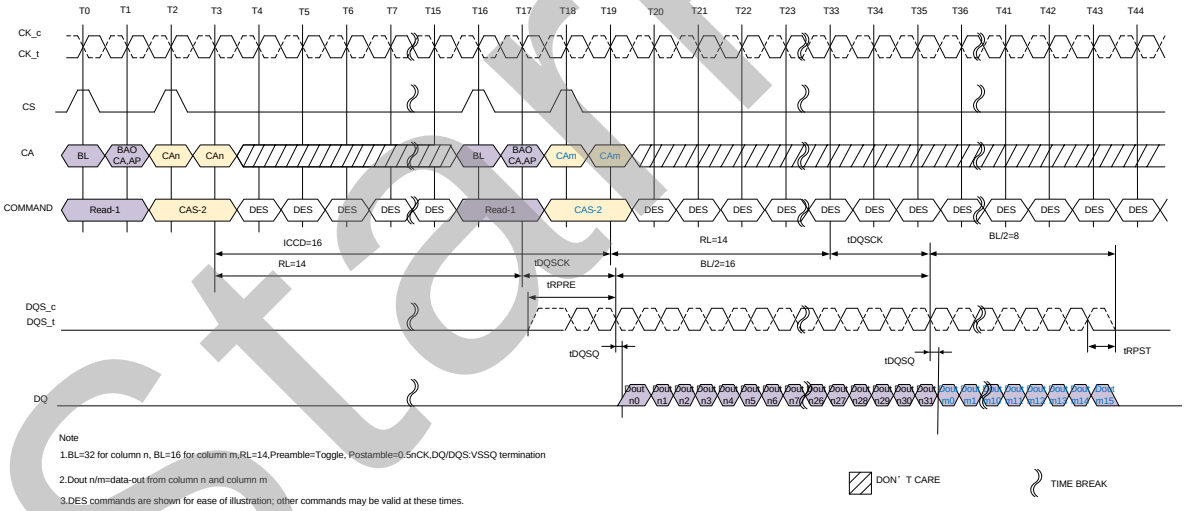
- WRITE Burst Operation WL=9(AL=0, CWL=9, BL8)



NOTE1 BL=8,WL=0,CWL=11,Preamble=1tCK
NOTE2 DOUTn=data-in to column n.
NOTE3 DES commands are shown for ease of illustration;other commands may be valid at these times.
NOTE4 BL8 setting activated by either MR0[A1:A0=00]or MR0[A1:A0=01]and A12=1 during WRITE command at T0.
NOTE5 CA Parity=Disable,CS to CA Latency = Disable, Write DBI= Disable .

Figure 10-2 DDR Write Burst Operation

- LPDDR4
  - Burst Read



Note
1.BL=32 for column n, BL=16 for column m,RL=14,Preamble=Toggle, Postamble=0.5nCK,DQ/DQS:VSSQ termination
2.Dout n/m=data-out from column n and column m
3.DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 10-3 LPDDR4 Burst Read

- Burst Write

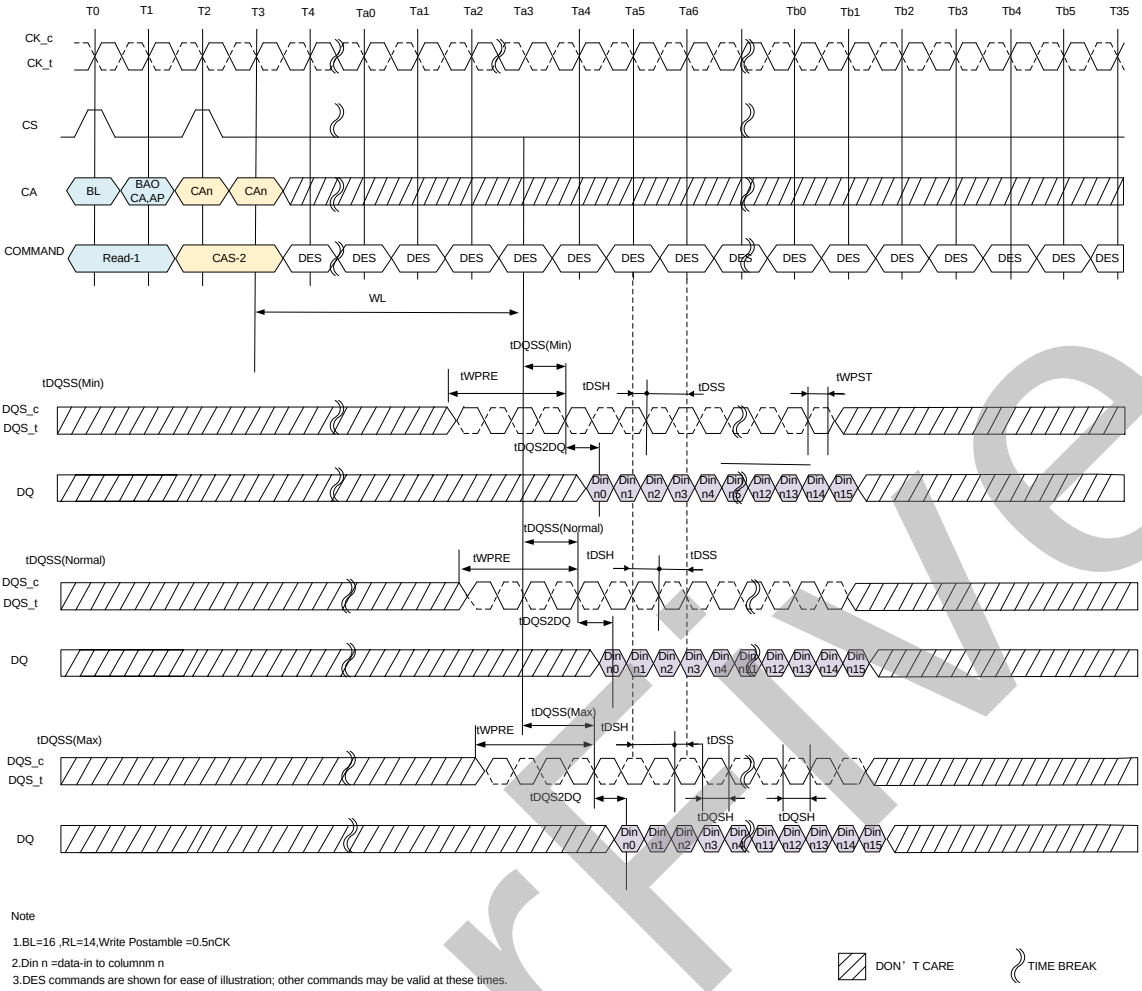


Figure 10-4 LPDDR4 Burst Write

- LPDDR3
  - Burst Read: RL=12, BL=8, $t_{DQSCK} > t_{CK}$

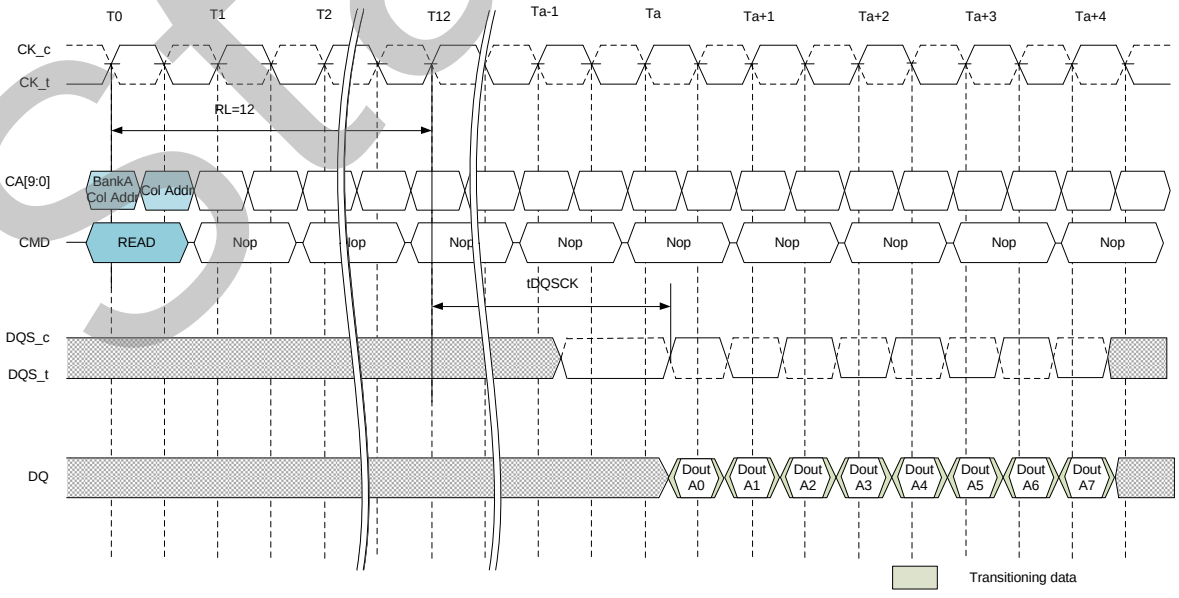


Figure 10-5 LPDDR3 Burst Read

- Burst Write

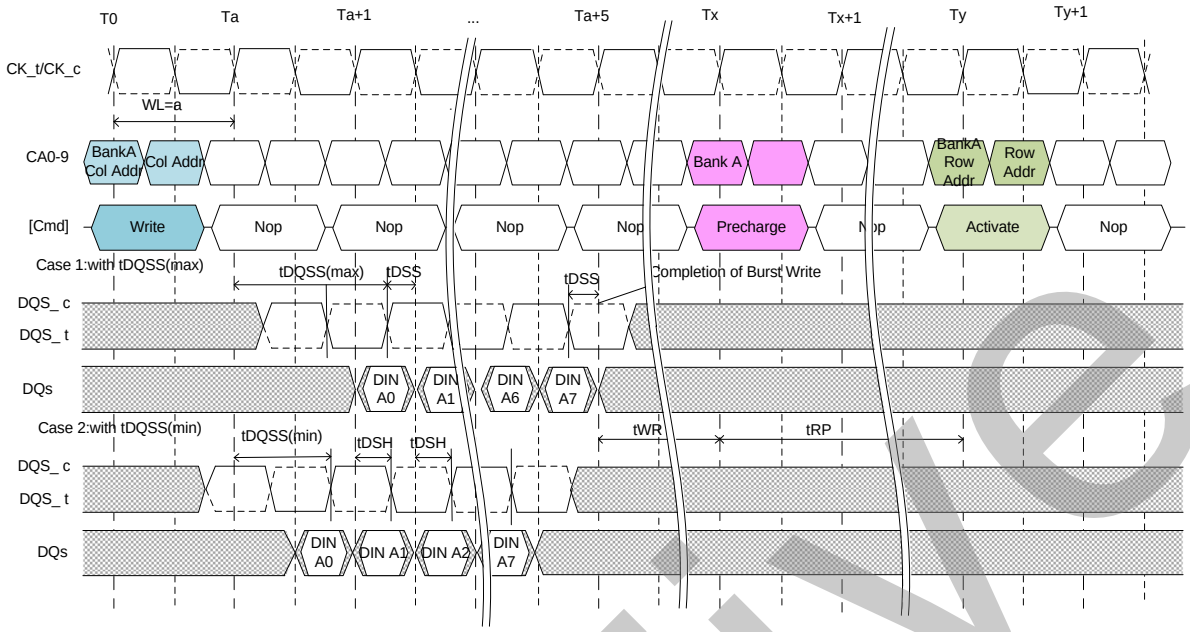


Figure 10-6 LPDDR3 Burst Write

10.2 RGMII Interface and Timing

- RGMII Transmit

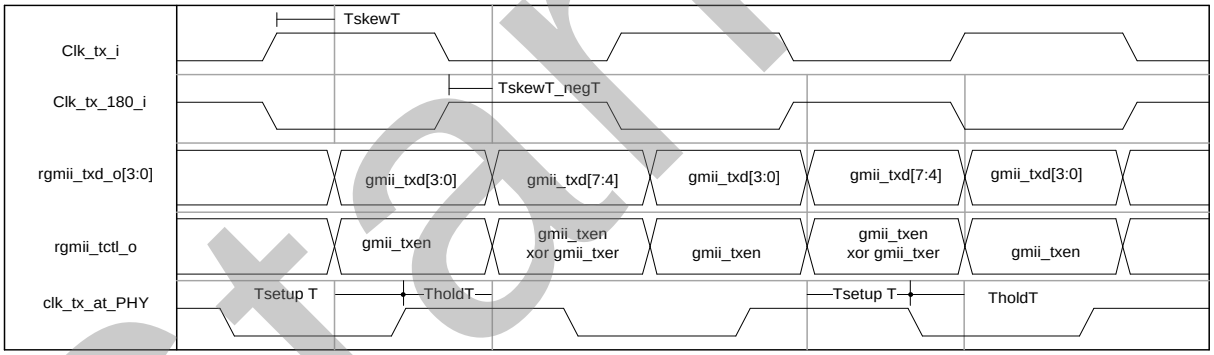


Figure 10-7 RGMII Transmit

- RGMII Receive

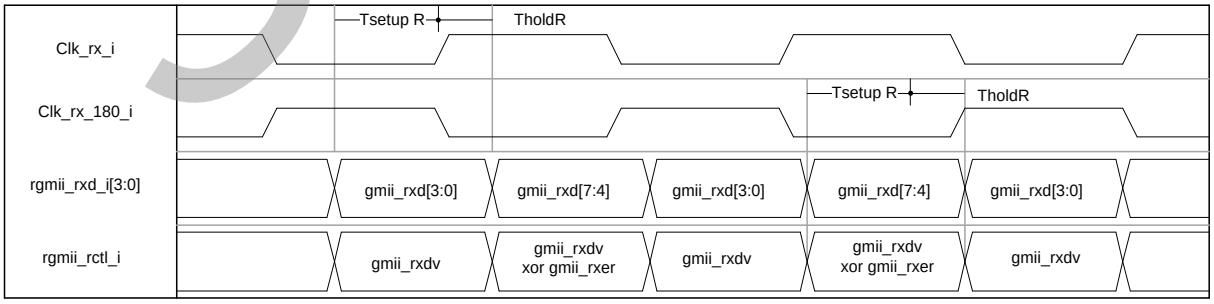


Figure 10-8 RGMII Receive

10.3 ChipLink Interface and Timing

- ChipLink Tx

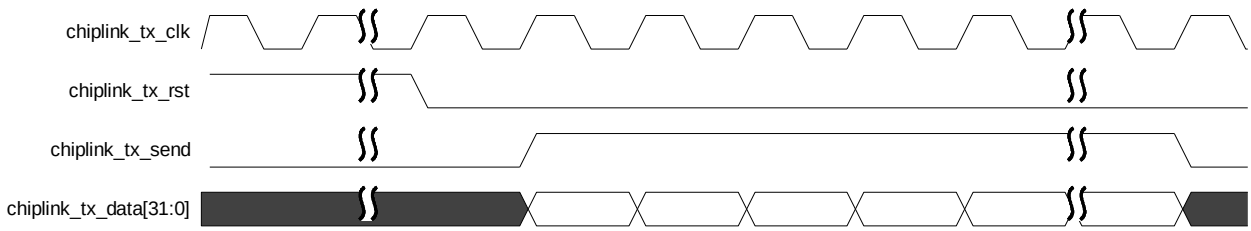


Figure 10-9 ChipLink TX

- ChipLink Rx

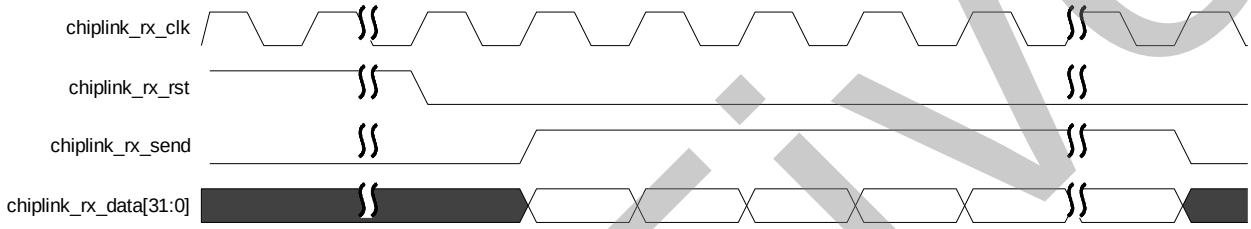


Figure 10-10 ChipLink RX

10.4 QSPI Interface and Timing

- Quad Output Fast Read Array (6Bh/6Ch)

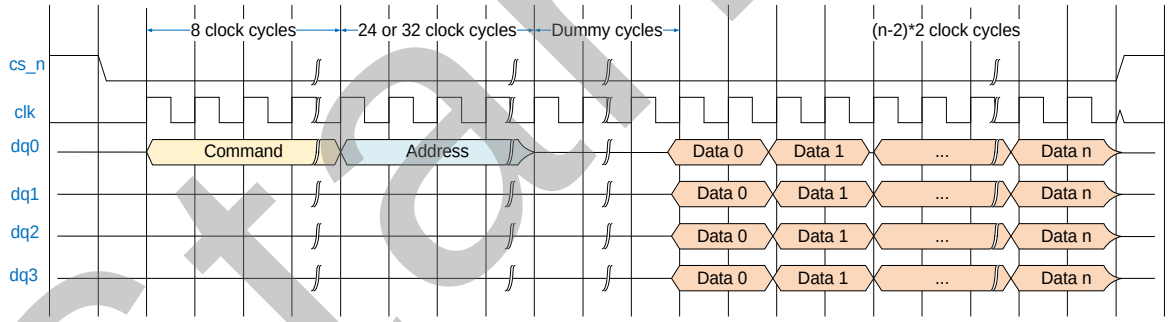


Figure 10-11 QSPI Fast read

- Quad Input Fast Byte/Page Program (32h/34h)

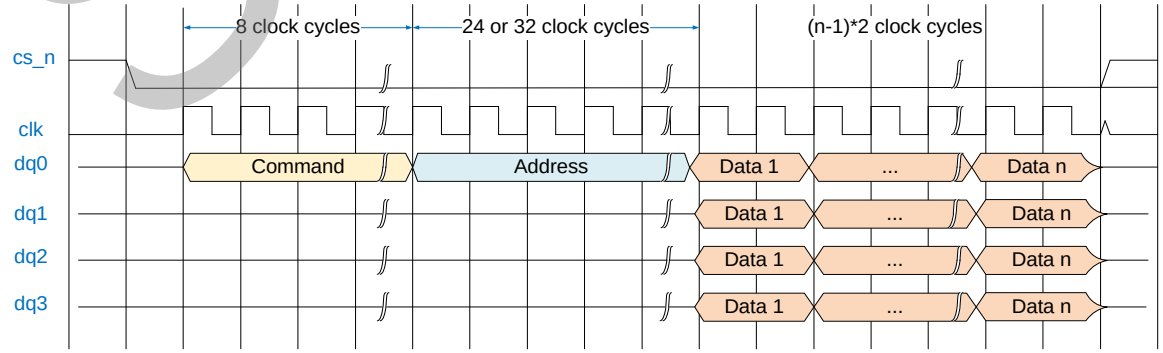


Figure 10-12 QSPI Fast Byte/Page Program

10.5 SPI Interface and Timing

- SPI Read

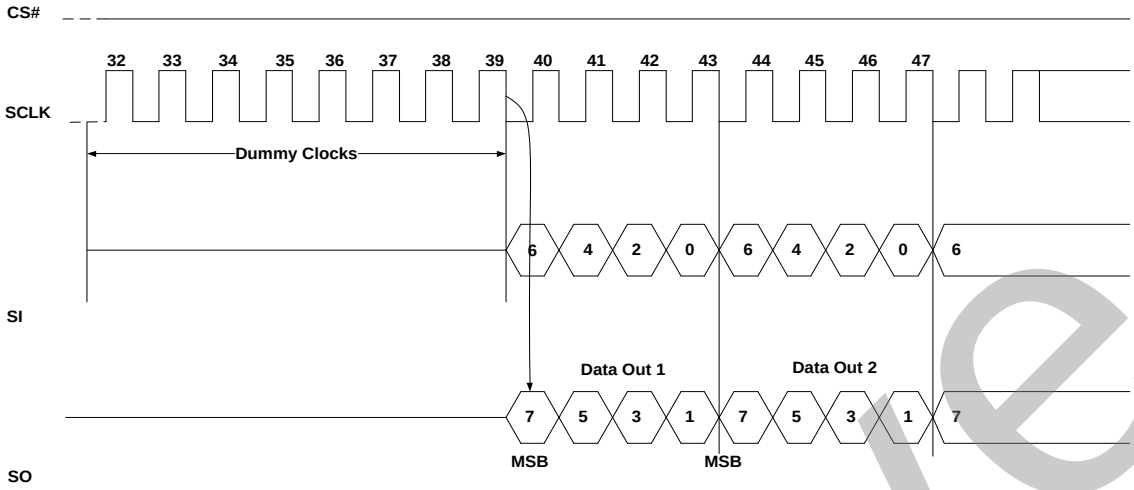


Figure 10-13 SPI Read

- SPI Write

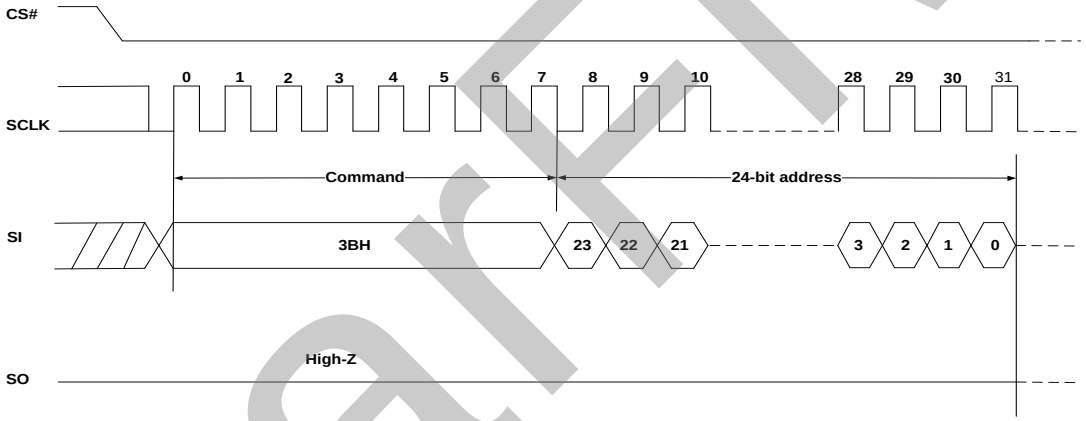


Figure 10-14 SPI Write

10.6 I2C Interface and Timing

- Data transfer on the I2C Bus

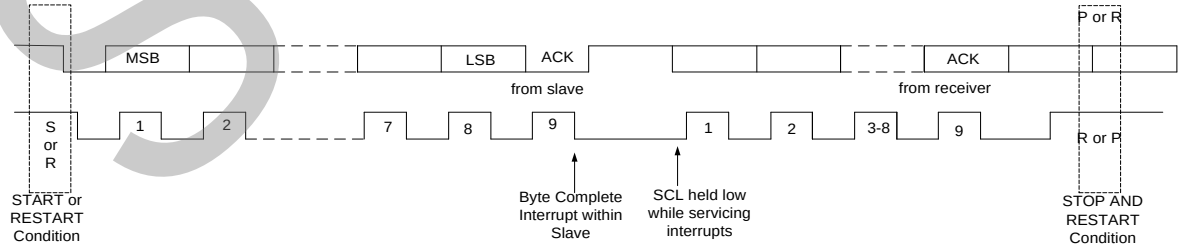


Figure 10-15 I2C Bus

11 Electrical Parameters

11.1 Absolute Maximum Ratings

Table 11-1 Absolute Maximum Ratings

Symbol	Parameters	Min	Max	Units
VDD	Power supply for Core	0.81	0.99	V
VDDIO	Power supply for Post-Driver	1.62	1.98	V
VDD3318	Power supply for 18OD33 IO Post-Driver	1.71	3.465	V
Vimax	Maximum Input Voltage	-	1.98	V
VDDramp-upslew	Ramp up slew for VDD	-	0.018	V/us
VDDIOramp-upslew	Ramp up slew for VDDIO	-	0.018	V/us
Tj	Junction Temperature	-40	125	℃
Ts	Storage temperature	0	70	℃

11.2 Recommended Operating Conditions

Table 11-2 Recommended Operating Conditions

Power	Ground	Description	Voltage			
			Min	Nom	Max	Units
VDD	VSS	Core power supply	0.81	0.9	0.99	V
VDD18		Digital IO power supply	1.62	1.8	1.98	V
VDD3318_CHIPLINK		FUNC_SHARE [0-69] IO power supply	3.135	3.3	3.465	V
VDD3318_LCD		FUNC_SHARE [70-97] IO power supply	3.135	3.3	3.465	V
VDD3318_SENSOR		FUNC_SHARE [98-114] IO power supply	3.135	3.3	3.465	V
VDD3318_GMII		FUNC_SHARE [115-141] IO power supply	3.135	3.3	3.465	V
AVDD18_MIPITX	VSS	MIPI TX analog power supply	1.62	1.8	1.98	V
AVDD18_MIPIRX	AVSS_MIPIRX	MIPI RX analog power supply	1.62	1.8	1.98	V

Power		Ground	Description	Voltage			
				Min	Nom	Max	Units
			for LDO				
AVDD09_MIPIRX			MIPI RX analog power supply	0.855	0.9	0.99	V
AVDD18_TS		VSS18_TS	Temperature sensor analog power supply	1.62	1.8	1.98	V
AVDD33_USB		AVSS_USB	USB analog power supply	2.97	3.3	3.63	V
AVDD18_USB			USB analog power supply	1.62	1.8	1.98	V
AVDD09TX_USB		AVSSTX_USB	USB TX analog power supply	0.85	0.9	0.95	V
AVDD09RX_USB		AVSSRX_USB	USB RX analog power supply	0.85	0.9	0.95	V
DVDD18_OTP		VSS18_OTP	OTP power supply	1.62	1.8	1.98	V
AVDD09_PLL0		AVSS_PLL0	PLL0 analog power supply	0.81	0.9	0.99	V
AVDD09_PLL1		AVSS_PLL1	PLL1 analog power supply	0.81	0.9	0.99	V
AVDD09_PLL2		AVSS_PLL2	PLL2 analog power supply	0.81	0.9	0.99	V
DDR4/LPDDR4	VDDPLL_DDR0	VSS	DDR0 PLL power supply	0.81	0.9	0.99	V
	VDDQ_DDR0		DDR0 IO power supply	1.14/1.06	1.2/1.1	1.26/1.17	V
	VDDQCK_DDR0		DDR0 CK power supply	1.14/1.06	1.2/1.1	1.26/1.17	V
	VDDPLL_DDR1		DDR1 PLL power supply	0.81	0.9	0.99	V
	VDDQ_DDR1		DDR1 IO power supply	1.14/1.06	1.2/1.1	1.26/1.17	V
	VDDQCK_DDR1		DDR1 CK power supply	1.14/1.06	1.2/1.1	1.26/1.17	V
DDR3/LPDDR3	VDDPLL_DDR0	VSS	DDR0 PLL power supply	0.81	0.9	0.99	V
	VDDQ_DDR0		DDR0 IO power supply	1.425/1.14	1.5/1.2	1.575/1.3	V
	VDDQCK_DDR0		DDR0 CK power supply	1.425/1.14	1.5/1.2	1.575/1.3	V
	VDDPLL_DDR1		DDR1 PLL power supply	0.81	0.9	0.99	V
	VDDQ_DDR1		DDR1 IO power supply	1.425/1.14	1.5/1.2	1.575/1.3	V
	VDDQCK_DDR1		DDR1 CK power supply	1.425/1.14	1.5/1.2	1.575/1.3	V

11.3 DC Characteristics

Table 11-3 DC Characteristics (1.8 IO, VDDIO=1.8V)

Symbol	Parameters	Min	Nom	Max	Units
VIL	Input Low Voltage	-0.3	-	0.35*VDDIO	V
VIH	Input High Voltage	0.65*VDDIO	-	1.98	V
VT	Threshold Point	0.82	0.89	0.97	V
Ii	Input Leakage Current @Vi=1.8V or 0V	-	-	±10u	A
Ioz	Tri-state Output Leakage Current @Vi=1.8V or 0V	-	-	±10u	A
Rpu	Pull-up Resistor	60k	89k	137k	Ω
Rpd	Pull-down Resistor	61k	104k	196k	Ω
VOL	Output Low Voltage	-	-	0.45	V
VOH	Output High Voltage	1.35	-	-	V
IOL	Low Level Output Current @VOL(max)	16.5	27	37.7	mA
IOH	High Level Output Current @VOH(min)	19.5	28.5	39	mA

Table 11-4 DC Characteristics (18OD33 IO, VDD3318=3.3V)

Symbol	Parameters	Min	Nom	Max	Units
VIL	Input Low Voltage	-0.3	-	0.8	V
VIH	Input High Voltage	2.0	-	3.465	V
VT	Threshold Point	1.02	1.17	1.36	V
Ii	Input Leakage Current @Vi=3.3V or 0V	-	-	±10u	A
Ioz	Tri-state Output Leakage Current @Vi=3.3V or 0V	-	-	±10u	A
Rpu	Pull-up Resistor	26k	46k	71k	Ω
Rpd	Pull-down Resistor	27k	48k	103k	Ω
VOL	Output Low Voltage	-	-	0.4	V
VOH	Output High Voltage	2.4	-	-	V
IOL	Low Level Output Current @VOL(max)				
	DS2, DS1, DS0=000	4.0	6.3	8.9	mA
	DS2, DS1, DS0=001	6.0	9.4	13.3	mA
	DS2, DS1, DS0=010	8.0	12.5	17.6	mA

Symbol	Parameters	Min	Nom	Max	Units
	DS2, DS1, DS0=011	9.9	15.5	21.8	mA
	DS2, DS1, DS0=100	11.9	18.6	26.1	mA
	DS2, DS1, DS0=101	13.9	21.6	30.2	mA
	DS2, DS1, DS0=110	15.8	24.5	34.2	mA
	DS2, DS1, DS0=111	17.7	27.4	38.1	mA
IOH	High Level Output Current @VOH(min)				
	DS2, DS1, DS0=000	5.9	9.3	14.2	mA
	DS2, DS1, DS0=001	8.8	13.9	21.2	mA
	DS2, DS1, DS0=010	11.7	18.5	28.2	mA
	DS2, DS1, DS0=011	14.6	23.1	35.2	mA
	DS2, DS1, DS0=100	17.5	27.7	42.2	mA
	DS2, DS1, DS0=101	20.3	32.2	49.1	mA
	DS2, DS1, DS0=110	23.2	36.8	56.0	mA
	DS2, DS1, DS0=111	26.1	41.3	62.8	mA

12 Supported Standards

12.1 LPDDR4/LPDDR3/DDR3/DDR4

- JESD209-3C
- JESD79-3D
- JESD79-4A
- JESD209-4B
- DFI 3.1 Specification
- Preliminary DFI 4.0 Specification Addendum to DFI 3.1

12.2 USB 2.0/3.0

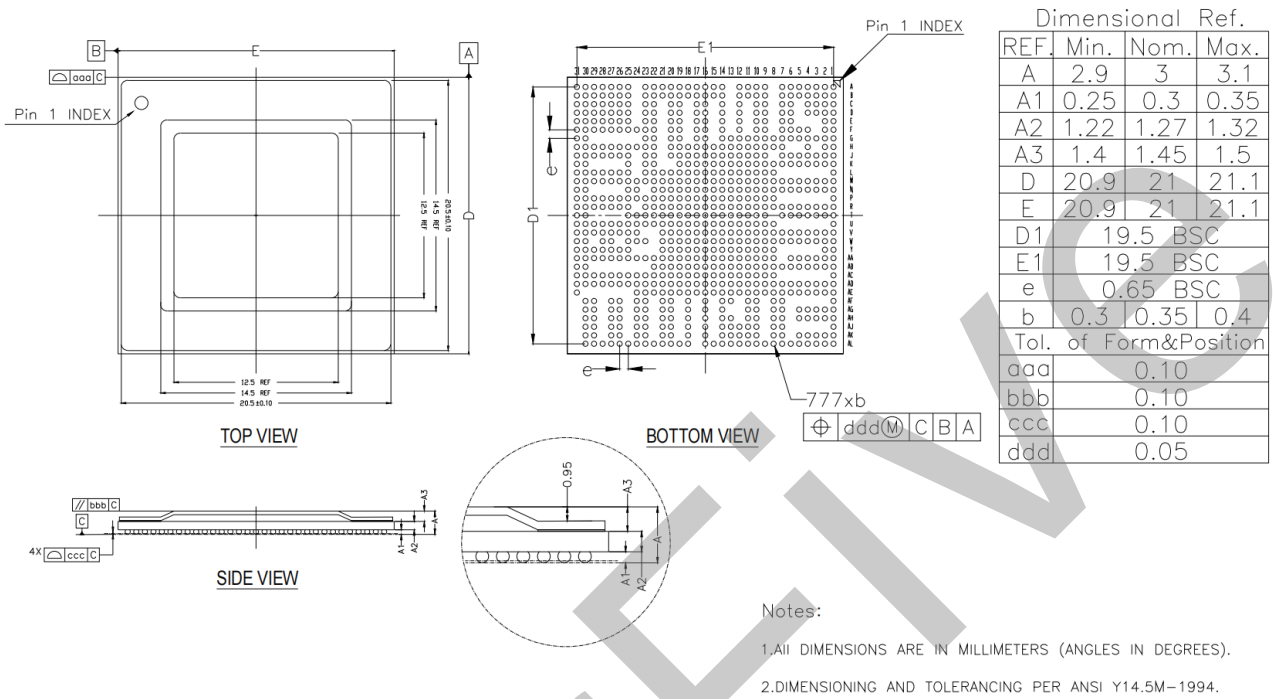
- USB-IF. On-The-Go and Embedded Host Supplement to USB Revision 2.0 Specification. July 27,2012. Revision 2.0 version 1.1a
- USB-IF. On-The-Go and Embedded Host Supplement to the USB Revision 3.0 Specification. May 10,2012. Revision 1.1
- Universal Serial Bus 3.0 Specification, Revision 1.0
- PHY Interface For the PCI Express and USB 3.0 Architectures. 2009
- Philips. UTMI+ Specification, Revision 1.0. 2004

12.3 Ethernet Mac

- IEEE 802.3-2008 standard Gigabit Media Independent Interface (GMII)
- IEEE 1588-2008 standard for precision networked clock synchronization
- IEEE 802.3az-2010, for Energy Efficient Ethernet (EEE)
- RMII specification version 1.2 from RMII consortium

13 Package Specification

The following figure shows the package outline of JH7100:



Dimensional Ref.

REF.	Min.	Nom.	Max.
A	2.9	3	3.1
A1	0.25	0.3	0.35
A2	1.22	1.27	1.32
A3	1.4	1.45	1.5
D	20.9	21	21.1
E	20.9	21	21.1
D1	19.5 BSC		
E1	19.5 BSC		
e	0.65 BSC		
b	0.3	0.35	0.4
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		

Figure 13-1 Package POD_FCBGA777